M4x.44xx-x4 - 14/16 bit Digitizer up to 500 MS/s

- **Up to 500 MS/s on four channels**
- **PXIe 3U format, 2 slots wide**
- **Ultra Fast PCI Express x4 Gen 2 interface**
- **Simultaneously sampling on all channels**
- **Separate dedicated ADC and amplifier per channel**
- **6 input ranges: ±200 mV up to ±10 V**
- **2 GSample (4 GByte) on-board memory**
- **Window, re-arm, OR/AND trigger**
- **Features: Single-Shot, Streaming, Multiple Recording, Gated Sampling, ABA, Timestamps**

Speed	SNR	ENOB
130 MS/s	up to 72.0 dB	up to 11.6 LSB
250 MS/s	up to 71.6 dB	up to 11.6 LSB
500 MS/s	up to 68.0 dB	up to 11.0 LSB

FPGA Options:

- Block Average up to 128k
- Block Statistics/Peak Detect

- PXIe x4 Gen 2 Interface
- Works with all PXIe and PXI hybrid slots
- Sustained streaming mode more than 1.7 GB/s**

Operating Systems

- Windows 7 (SP1), 8, 10, Server 2008 R2 and newer
- Linux Kernel 2.6, 3.x, 4.x, 5.x
- Windows/Linux 32 and 64 bit

Recommended Software

- Visual C++, C++ Builder, Delphi GNU C++, VB.NET, C#, J#, Java, Python
- SBench 6

Drivers

- MATLAB
- LabVIEW
- IVI

Model		1 channel	2 channels	4 channels
M4x.4451-x4	14 Bit	500 MS/s	500 MS/s	500 MS/s
M4x.4450-x4	14 Bit	500 MS/s	500 MS/s	
M4x.4421-x4	16 Bit	250 MS/s	250 MS/s	250 MS/s
M4x.4420-x4	16 Bit	250 MS/s	250 MS/s	
M4x.4411-x4	16 Bit	130 MS/s	130 MS/s	130 MS/s
M4x.4410-x4	16 Bit	130 MS/s	130 MS/s	

Export-Versions

Sampling rate restricted versions that do not fall under export restrictions.

Model		1 channel	2 channels	4 channels
M4x.4481-x4	14 Bit	400 MS/s	400 MS/s	400 MS/s
M4x.4480-x4	14 Bit	400 MS/s	400 MS/s	
M4x.4471-x4	16 Bit	180 MS/s	180 MS/s	180 MS/s
M4x.4470-x4	16 Bit	180 MS/s	180 MS/s	

General Information

The M4x.44xx-x4 series digitizers deliver the highest performance in both speed and resolution. The series includes PXIe cards with either two or four synchronous channels where each channel has its own dedicated ADC. The ADC's can sample at rates from 130 MS/s up to 500 MS/s and are available with either 14 bit or 16 bit resolution. The combination of high sampling rate and resolution makes these digitizers the top-of-the-range for applications that require high quality signal acquisition.
The PXIe digitizers feature a interface with PCI Express x4 Gen 2 interface that offers outstanding data streaming performance. The interface and Spectrum's optimized drivers enable data transfer rates in excess of 1.7 GB/s** so that signals can be acquired, stored and analyzed at the fastest speeds.
While the cards have been designed using the latest technology they are still software compatible with the drivers from earlier Spectrum digitizers. So, existing customers can use the same software they developed for a 10 year old 200 kS/s multi-channel card and for an M4x series 500 MS/s high resolution digitizer!

**Throughput measured with a motherboard chipset supporting a TLP size of 256 bytes.

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22.10.2020

Software Support

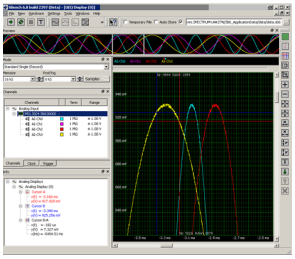
Windows drivers

The cards are delivered with drivers for Windows 7, Windows 8 and Windows 10 (32 bit and 64 bit). Programming examples for Visual C++, C++ Builder, Delphi, Visual Basic, VB.NET, C#, J#, Python, Java and IVI are included.

Linux Drivers

All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like Fedora, Suse, Ubuntu LTS or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for GNU C++, Python as well as the possibility to get the driver sources for your own compilation.

SBench 6



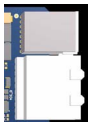
A base license of SBench 6, the easy-to-use graphical operating software for Spectrum cards, is included in the delivery. The base license makes it is possible to test the card, display acquired data and make some basic measurements. It's a valuable tool for checking the card's performance and assisting with the unit's initial setup. The cards also come with a demo license for the SBench 6 professional version. This license gives the user the opportunity to test the additional features of the professional version with their hardware. The professional version contains several advanced measurement functions, such as FFTs and X/Y display, import and export utilities as well as support for all acquisition modes including data streaming. Data streaming allows the cards to continuously acquire data and transfer it directly to the PC RAM or hard disk. SBench 6 has been optimized to handle data files of several GBytes. SBench 6 runs under Windows as well as Linux (KDE, GNOME and Unity) operating systems. A test version of SBench 6 can be downloaded directly over the internet and can run the professional version in a simulation mode without any hardware installed. Existing customers can also request a demo license for the professional version from Spectrum. More details on SBench 6 can be found in the SBench 6 data sheet.

Third-party products

Spectrum supports the most popular third-party software products such as LabVIEW, MATLAB or LabWindows/CVI. All drivers come with detailed documentation and working examples are included in the delivery. Support for other software packages, like VEE or DasyLab, can also be provided on request.

Hardware features and options

PXI Express x4

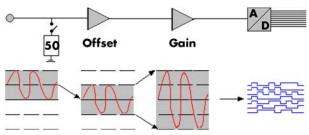


The M4x series PXI Express cards use a PCI Express x4 Gen 2 connection. They can be used in every PXI Express (PXIe) slot, as well as in any PXI hybrid slot with Gen 1, Gen 2 or Gen 3. The maximum sustained data transfer rate is more than 1.7 GByte/s (read direction) or 1.4 GByte/s (write direction) per slot.

Connections

- The cards are equipped with SMA connectors for the analog signals as well as for the two external trigger inputs, and clock input and output. In addition, there are three MMCX connectors that are used for the three multi-function I/O connectors. These multi-function connectors can be individually programmed to perform different functions:
- Trigger output
- Status output (armed, triggered, ready, ...)
- Synchronous digital inputs, being stored inside the analog data samples
- Asynchronous I/O lines

Input Amplifier



The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands the input termination can be changed between 50 Ohm and 1 MOhm, one can select a matching input range and the signal offset can be compensated by programmable AC coupling. The latest hardware revisions additionally allow for offset compensation for DC-coupled inputs as well.

Software selectable input path

For each of the analog channels the user has the choice between two analog input paths. The „Buffered" path offers the highest flexibility when it comes to input ranges and termination. A software programmable 50 Ohm and 1 MOhm termination also allows to connect standard oscilloscope probes to the card. The „50 Ohm" path on the other hand provides the highest bandwidth and the best signal integrity with a fewer number of input ranges and a fixed 50 Ohm termination.

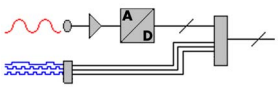
Software selectable lowpass filter

Each analog channel contains a software selectable low-pass filter to limit the input bandwidth. Reducing the analog input bandwidth results in a lower total noise and can be useful especially with low voltage input signals.

Automatic on-board calibration

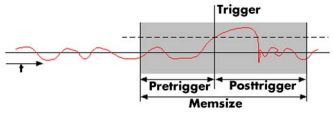
Every channel of each card is calibrated in the factory before the board is shipped. However, to compensate for environmental variations like PC power supply, temperature and aging the software driver includes routines for automatic offset and gain calibration. This calibration is performed on all input ranges of the "Buffered" path and uses a high precision onboard calibration reference.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. As standard a maximum of 3 additional digital inputs are available on the front plate of the card using the multi-purpose I/O lines. An additional option offers 8 more digital channels.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

FIFO mode

The FIFO or streaming mode is designed for continuous data transfer between the digitizer card and the PC memory. When mounted in a PXI Express x4 Gen 2 capable PXIe slot, read streaming speeds of up to 1.7 GByte/s are possible. The control of the data stream is done automatically by the driver on interrupt request basis. The complete installed onboard memory is used to buffer the data, making the continuous streaming process extremely reliable.

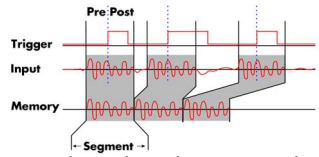
Channel trigger

The digitizers offer a wide variety of trigger modes. These include a standard triggering mode based on a signals level and slope, like that found in most oscilloscopes. It is also possible to define a window mode, with two trigger levels, that enables triggering when signals enter or exit the window. Each input has its own trigger circuit which can be used to setup conditional triggers based on logical AND/OR patterns. All trigger modes can be combined with a re-arming mode for accurate trigger recognition even on noisy signals.

External trigger input

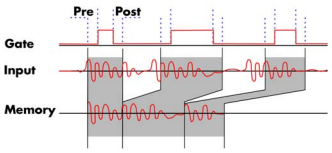
All boards can be triggered using up to two external analog or digital signals. One external trigger input has two analog comparators that can define an edge or window trigger, a hysteresis trigger or a rearm trigger. The other input has one comparator that can be used for standard edge and level triggers.

Multiple Recording



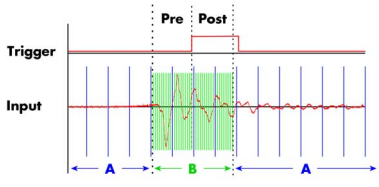
The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

Gated Sampling



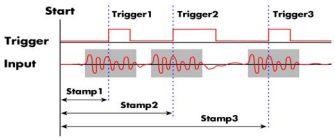
The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

ABA mode



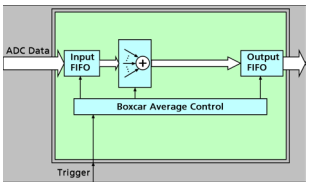
The ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

Timestamp



The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronized to a radio clock, an IRIG-B a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

Boxcar Average (high-resolution) mode

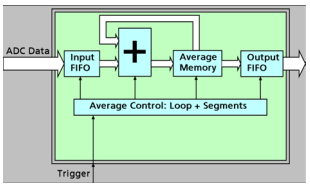


The Boxcar average or high-resolution mode is a form of averaging. The ADC oversamples the signal and averages neighboring points together. This mode uses a real-time boxcar averaging algorithm that helps reducing random noise. It also can yield a higher number of bits of resolution depening on the signal acquired. The averaging factor can be set in the region of 2 to 256. Averaged samples are stored as 32 bit values and can be processed by any software. The trigger detection is still running with full sampling speed allowing a very precise relation between acquired signal and the trigger.

8bit Sample reduction (low-resolution) mode

The cards and digitizerNETBOXes of the 44xx series allow to optionally reduce the resolution of the A/D samples from their native 14 bit or 16 bit down to 8bit resolution, such that each sample will only occupy one byte in memory instead of the standard two bytes required. This does not only enhance the size of the on-board memory from 2 GSamples to effectively 4 Gsamples, but also reduces the required bandwidth over the PCIe bus and also to the storage devices, such as SSD or HDD.

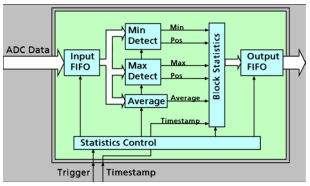
Firmware Option Block Average



The Block Average Module improves the fidelity of noisy repetitive signals. Multiple repetitive acquisitions with very small dead-time are accumulated and averaged. Random noise is reduced by the averaging process improving the visibility of the repetitive signal. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

Please see separate data sheet for details on the firmware option.

Firmware Option Block Statistics (Peak Detect)



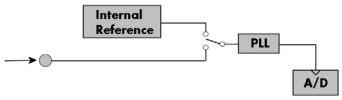
The Block Statistics and Peak Detect Module implements a widely used data analysis and reduction technology in hardware. Each block is scanned for minimum and maximum peak and a summary including minimum, maximum, average, timestamps and position information is stored in memory. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

Please see separate data sheet for details on the firmware option.

External clock input and output

Using a dedicated connector a sampling clock can be fed in from an external system. Additionally it's also possible to output the internally used sampling clock on a separate connector to synchronize external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

PXIe bus

The PXI Express bus (PCI Express eXtension for instrumentation) offers a variety of additional normed possibilities for synchronising different components in one system. It is posible to connect several Spectrum cards with each other as well as to connect a Spectrum card with cards of other manufacturers.

PXI reference clock

The card is able to use the 100 MHz low-jitter reference clock that is supplied by the PXIe system. Enabled by software the PXIe reference clock is fed into the on-board PLL. This feature allows the cards to run with a fixed phase relation.

PXI trigger

The Spectrum cards support star trigger as well as the PXI trigger bus. Using a simple software commend one or more trigger lines can be used as trigger source. This feature allows the easy setup of OR connected triggers from different cards.

External Amplifiers

For the acquisition of extremely small voltage levels with a high bandwidth a series of external amplifiers is available. Each of the one channel amplifiers is working with a fixed input impedance and allows - depending on the bandwidth - to select different amplification levels between x10 (20 dB) up to x1000 (60 dB). Using the external amplifiers of the SPA series voltage levels in the uV and mV area can be acquired.

Export Versions

Special export versions of the products are available that do not fall under export control. Products fall under export control if their specification exceeds certain sampling rates at a given A/D resolution and if the product is shipped into a country where no general export authorization is in place.

The export versions of the products have a sampling rate limitation matching the export control list. An upgrade to the faster version is not possible. The sampling rate limitation is in place for both internal and external clock.

Technical Data

Analog Inputs

Resolution	130 MS/s up to 250 MS/s 400 MS/s and 500 MS/s	16 bit (441, 442, 447) 14 bit (445, 448)	
Input Type		Single-ended	
ADC Differential non linearity (DNL)	ADC only	±0.5 LSB (14 Bit ADC), ±0.4 LSB (16 Bit ADC)	
ADC Integral non linearity (INL)	ADC only	±2.5 LSB (14 Bit ADC), ±10.0 LSB (16 Bit ADC)	
ADC Word Error Rate (WER)	max. sampling rate	10^{-12}	
Channel selection	software programmable	1, 2, or 4 (maximum is model dependent)	
Bandwidth filter	activate by software	20 MHz bandwidth with 3rd order Butterworth filtering	
Input Path Types	software programmable	**50 Ω (HF) Path**	**Buffered (high impedance) Path**
Analog Input impedance	software programmable	50 Ω	1 MΩ || 25 pF or 50 Ω
Input Ranges	software programmable	±500 mV, ±1 V, ±2.5 V, ±5 V	±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Programmable Input Offset	Frontend HW-Version < V9	not available	not available
Programmable Input Offset	Frontend HW-Version >= V9	–100%..0% on all ranges	–100%..0% on all ranges except ±1 V and ±10 V
Input Coupling	software programmable	AC/DC	AC/DC
Offset error (full speed)	after warm-up and calibration	< 0.1% of range	< 0.1% of range
Gain error (full speed)	after warm-up and calibration	< 1.0% of reading	< 1.0% of reading
Over voltage protection	range ≤ ±1V	2 Vrms	±5 V (1 MΩ), 5 Vrms (50 Ω)
Over voltage protection	range ≥ ±2V	6 Vrms	±30 V (1 MΩ), 5 Vrms (50 Ω)
Max DC voltage if AC coupling active		±30 V	±30 V
Relative input stage delay		Bandwidth filter disabled: 0 ns Bandwidth filter enabled: 14.7 ns	Bandwidth filter disabled: 3.8 ns Bandwidth filter enabled: 18.5 ns
Crosstalk 1 MHz sine signal	range ±1V	≤96 dB	≤93 dB
Crosstalk 20 MHz sine signal	range ±1V	≤82 dB	≤82 dB
Crosstalk 1 MHz sine signal	range ±5V	≤97 dB	≤85 dB
Crosstalk 20 MHz sine signal	range ±5V	≤82 dB	≤82 dB

	M4i.441x M4x.441x DN2.441-xx DN6.441-xx	M4i.442x M4x.442x DN2.442-xx DN6.442-xx	M4i.445x M4x.445x DN2.445-xx DN6.445-xx	M4i.447x M4x.447x DN2.447-xx DN6.447-xx	M4i.448x M4x.448x DN2.448-xx DN6.448-xx
lower bandwidth limit (DC coupling)	0 Hz	0 Hz	0 Hz	0 Hz	0 Hz
lower bandwidth limit (AC coupled, 50 Ω)	< 30 kHz	< 30 kHz	< 30 kHz	< 30 kHz	< 30 kHz
lower bandwidth limit (AC coupled, 1 MΩ)	< 2 Hz	< 2 Hz	< 2 Hz	< 2 Hz	< 2 Hz
-3 dB bandwidth (HF path, AC coupled, 50 Ω)	65 MHz	125 MHz	250 MHz	125 MHz	250 MHz
Flatness within ±0.5 dB (HF path, AC coupled, 50 Ω)	40 MHz	80 MHz	160 MHz	80 MHz	160 MHz
-3 dB bandwidth (Buffered path, DC coupled, 1 MΩ)	50 MHz	85 MHz	85 MHz (V1.1) 125 MHz (V1.2)	85 MHz	125 MHz (V1.2)
-3 dB bandwidth (bandwidth filter enabled)	20 MHz	20 MHz	20 MHz	20 MHz	20 MHz

Trigger

Available trigger modes	software programmable	Channel Trigger, External, Software, Window, Re-Arm, Or/And, Delay, PXI (M4x only)	
Channel trigger level resolution	software programmable	14 bit	
Trigger engines		1 engine per channel with two individual levels, 2 external triggers	
Trigger edge	software programmable	Rising edge, falling edge or both edges	
Trigger delay	software programmable	0 to (8GSamples - 16) = 8589934576 Samples in steps of 16 samples	
Multi, Gate, ABA: re-arming time		40 samples (+ programmed pretrigger)	
Pretrigger at Multi, ABA, Gate, FIFO, Boxcar	software programmable	16 up to [8192 Samples in steps of 16)	
Posttrigger	software programmable	16 up to 8G samples in steps of 16 (defining pretrigger in standard scope mode)	
Memory depth	software programmable	32 up to [installed memory / number of active channels] samples in steps of 16	
Multiple Recording/ABA segment size, Boxcar	software programmable	32 up to [installed memory / 2 / active channels] samples in steps of 16	
Trigger accuracy (all sources)		1 sample	
Boxcar (high-resolution) average factor	software programmable	2, 4, 8, 16, 32, 64, 128 or 256	
Timestamp modes	software programmable	Standard, Startreset, external reference clock on X0 (e.g. PPS from GPS, IRIG-B)	
Data format		Std., Startreset:	64 bit counter, increments with sample clock (reset manually or on start)
		RefClock:	24 bit upper counter (increment with RefClock) 40 bit lower counter (increments with sample clock, reset with RefClock)
Extra data	software programmable	none, acquisition of X0/X1/X2 inputs at trigger time, trigger source (for OR trigger)	
Size per stamp		128 bit = 16 bytes	

External trigger		**Ext0**	**Ext1**
External trigger impedance	software programmable	50 Ω /1 kΩ	1 kΩ
External trigger coupling	software programmable	AC or DC	fixed DC
External trigger type		Window comparator	Single level comparator
External input level		±10 V (1 kΩ), ±2.5 V (50 Ω),	±10 V
External trigger sensitivity (minimum required signal swing)		2.5% of full scale range	2.5% of full scale range = 0.5 V
External trigger level	software programmable	±10 V in steps of 10 mV	±10 V in steps of 10 mV
External trigger maximum voltage		±30V	±30 V
External trigger bandwidth DC	50 Ω 1 kΩ	DC to 200 MHz DC to 150 MHz	n.a. DC to 200 MHz
External trigger bandwidth AC	50 Ω	20 kHz to 200 MHz	n.a.
Minimum external trigger pulse width		≥ 2 samples	≥ 2 samples

Clock

Clock Modes	software programmable	internal PLL, external reference clock, Star-Hub sync (M4i only), PXI Reference Clock (M4x only)
Internal clock accuracy		≤ ±20 ppm
Internal clock setup granularity	standard clock mode	divider: maximum sampling rate divided by: 1, 2, 4, 8, 16, ... up to 131072 (full gain accuracy)
Internal clock setup granularity	special clock mode only	1 Hz (reduced gain accuracy when using special clock mode), only available for single cards (no star-hub), only available for DigitizerNETBOX with one internal digitizer.
Clock setup range gaps	special clock mode only	unsetable clock speeds: 17.5 MHz to 17.9 MHz, 35.1 MHz to 35.8 MHz, 70 MHz to 72 MHz, 140 MHz to 144 MHz, 281 MHz to 287 MHz
External reference clock range	software programmable	≥ 10 MHz and ≤ 1 GHz
External reference clock input impedance		50 Ω fixed
External reference clock input coupling		AC coupling
External reference clock input edge		Rising edge
External reference clock input type		Single-ended, sine wave or square wave
External reference clock input swing	square wave	0.3 V peak-peak up to 3.0 V peak-peak
External reference clock input swing	sine wave	1.0 V peak-peak up to 3.0 V peak-peak
External reference clock input max DC voltage		±30 V (with max 3.0 V difference between low and high level)
External reference clock input duty cycle requirement		45% to 55%
Internal ADC clock output type		Single-ended, 3.3V LVPECL
Internal ADC clock output frequency	standard clock mode	Fixed to maximum sampling rate (500 MS/s, 250 MS/s or 130 MS/s depending on type)
Internal ADC clock output frequency	special clock mode	445x models (500 MS/s): ADC clock in the range between 80 MS/s and 500 MS/s 448x models (400 MS/s): ADC clock in the range between 80 MS/s and 400 MS/s 442x models (250 MS/s): ADC clock in the range between 40 MS/s and 250 MS/s 447x models (180 MS/s): ADC clock in the range between 40 MS/s and 180 MS/s 441x models (130 MS/s): ADC clock in the range between 40 MS/s and 130 MS/s
Star-Hub synchronization clock modes	software selectable	Standard clock mode with internal reference (maxmimum clock + divider), Standard clock mode with external reference (maxmimum clock + divider) special clock mode not allowed, except: 445 series (500 MS/s) can also run with 400 MS/s and divided clock for synchronization 442 series (250 MS/s) can also run with 180 MS/s and divided clock for synchronization
ABA mode clock divider for slow clock	software programmable	16 up to (128k - 16) in steps of 16
Channel to channel skew on one card		< 60 ps (typical)
Skew between star-hub synchronized cards		< 130 ps (typical, preliminary)

	M4i.441x M4x.441x DN2.441-xx DN6.441-xx	M4i.442x M4x.442x DN2.442-xx DN6.442-xx	M4i.445x M4x.445x DN2.445-xx DN6.445-xx	M4i.447x M4x.447x DN2.447-xx DN6.447-xx	M4i.448x M4x.448x DN2.448-xx DN6.448-xx
ADC Resolution	16 bit	16 bit	14 bit	16 bit	14 bit
max sampling clock	130 MS/s	250 MS/s	500 MS/s	180 MS/s	400 MS/s
min sampling clock (standard clock mode)	3.814 kS/s	3.814 kS/s	3.814 kS/s	3.814 kS/s	3.814 kS/s
min sampling clock (special clock mode)	0.610 kS/s	0.610 kS/s	0.610 kS/s	0.610 kS/s	0.610 kS/s

Block Average Signal Processing Option M4i.44xx/M4x.44xx/DN2.44x/DN6.44x Series

		Firmware ≥ V1.14 (since August 2015)	Firmware < V1.14
Minimum Waveform Length		32 samples	32 samples
Minimum Waveform Stepsize		16 samples	16 samples
Maximum Waveform Length	1 channel active	128 kSamples	32 kSamples
Maximum Waveform Length	2 channels active	64 kSamples	16 kSamples
Maximum Waveform Length	4 or more channels active	32 kSamples	8 kSamples
Minimum Number of Averages		2	2
Maximum Number of Averages		65536 (64k)	65536 (64k)
Data Output Format	fixed	32 bit signed integer	32 bit signed integer
Re-Arming Time between waveforms		40 samples (+ programmed pretrigger)	40 samples (+ programmed pretrigger)
Re-Arming Time between end of average to start of next average		Depending on programmed segment length, max 100 µs	40 samples (+ programmed pretrigger)

Block Statistics Signal Processing Option M4i.44xx/M4x.44xx/DN2.44x/DN6.44x Series

Minimum Waveform Length		32 samples
Minimum Waveform Stepsize		16 samples
Maximum Waveform Length	Standard Acquisition	2 GSamples / channels
Maximum Waveform Length	FIFO Acquisition	2 GSamples
Data Output Format	fixed	32 bytes statistics summary
Statistics Information Set per Waveform		Average, Minimum, Maximum, Position Minimum, Position Maximum, Trigger Timestamp
Re-Arming Time between Segments		40 samples (+ programmed pretrigger)

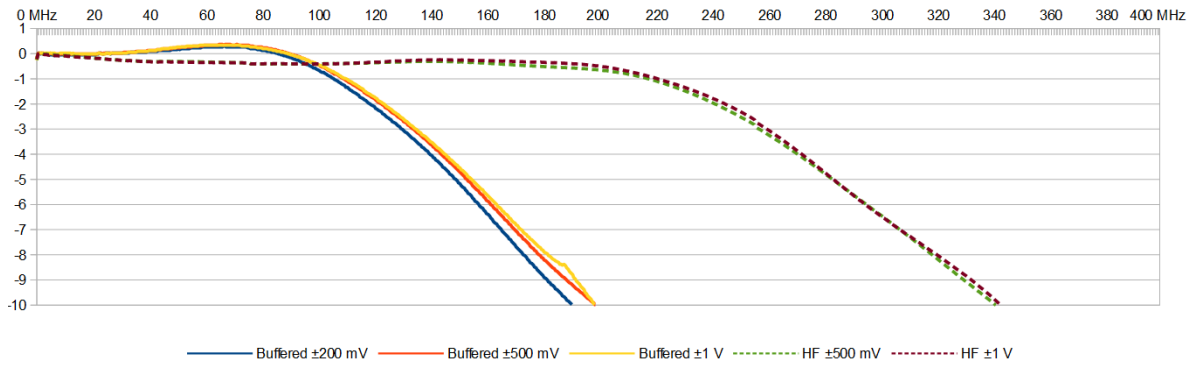
Multi Purpose I/O lines (front-plate)

Number of multi purpose lines		three, named X0, X1, X2
Input: available signal types	software programmable	Asynchronous Digital-In, Synchronous Digital-In, Timestamp Reference Clock
Input: impedance		10 kΩ to 3.3 V
Input: maximum voltage level		-0.5 V to +4.0 V
Input: signal levels		3.3 V LVTTL
Input: bandwith		125 MHz
Output: available signal types	software programmable	Asynchronous Digital-Out, Trigger Output, Run, Arm, PLL Refclock, System Clock
Output: impedance		50 Ω
Output: signal levels		3.3 V LVTTL
Output: type		3.3V LVTTL, TTL compatible for high impedance loads
Output: drive strength		Capable of driving 50 Ω loads, maximum drive strength ±48 mA
Output: update rate	14bit or 16 bit ADC resolution	sampling clock
Output: update rate	7 bit or 8 bit ADC resolution	Current sampling clock ≤ 1.25 GS/s : sampling clock Current sampling clock > 1.25 GS/s and ≤ 2.50 GS/s : ½ sampling clock Current sampling clock > 2.50 GS/s and ≤ 5.00 GS/s : ¼ sampling clock

Frequency Response Plots

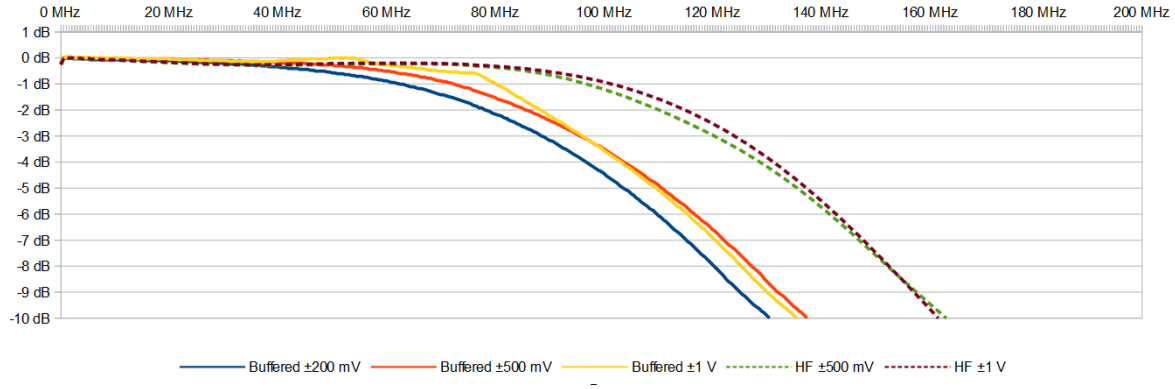
Frequency Response M4i.445x, M4x.445x, DN2.445-xx and DN6.445-xx

Sampling Rate 500 MS/s
HF Path 50 Ω, AC coupling, no filter
Buffered Path 1 MΩ, AC Coupling, no filter



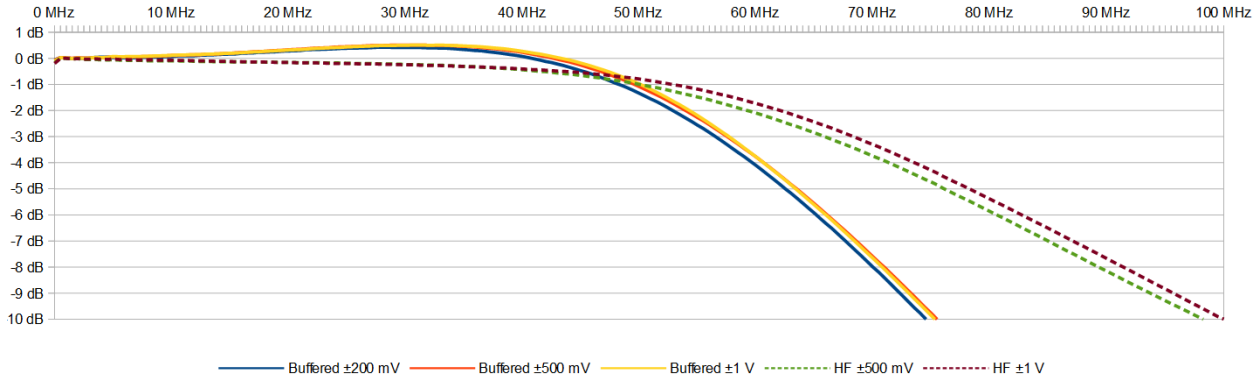
Frequency Response M4i.442x, M4x.442x, DN2.442-xx and DN6.442-xx

Sampling Rate 250 MS/s
HF Path 50 Ω, AC coupling, no filter
Buffered Path 1 MΩ, AC Coupling, no filter



Frequency Response M4i.441x, M4x.441x, DN2.441-xx and DN6.441-xx

Sampling Rate 130 MS/s
HF Path 50 Ω, AC coupling, no filter
Buffered Path 1 MΩ, AC Coupling, no filter



RMS Noise Level (Zero Noise), typical figures

M4i.445x, M4x.445x, DN2.445-xx and DN6.445-xx, 14 Bit 500 MS/s
M4i.448x, M4x.448x, DN2.448-xxx and DN6.448-xx, 14 Bit 400 MS/s

Input Range	±200 mV		±500 mV		±1		±2 V		±2.5 V		±5 V		±10 V	
Voltage resolution	24.4 µV		61.0 µV		122.1 µV		244.1 µV		305.2 µV		610.4 µV		1.22 mV	
HF path, DC, fixed 50 Ω			<1.9 LSB	<116 µV	<1.9 LSB	<232 µV			<1.9 LSB	<580 µV	<1.9 LSB	<1.16 mV		
Buffered path, full bandwidth	<3.8 LSB	<93 µV	<2.7 LSB	<165 µV	<2.1 LSB	<256 µV	<3.8 LSB	<928 µV			<2.7 LSB	<1.65 mV	<2.0 LSB	<2.44 mV
Buffered path, BW limit active	<2.2 LSB	<54 µV	<2.0 LSB	<122 µV	<2.0 LSB	<244 µV	<3.2 LSB	<781 µV			<2.3 LSB	<1.40 mV	<2.0 LSB	<2.44 mV

M4i.442x, M4x.442x, DN2.442-xx and DN6.442-xx, 16 Bit 250 MS/s
M4i.447x, M4x.447x, DN2.447-xx and DN6.447-xx, 16 Bit 180 MS/s

Input Range	±200 mV		±500 mV		±1		±2 V		±2.5 V		±5 V		±10 V	
Voltage resolution	6.1 µV		15.3 µV		30.5 µV		61.0 µV		76.3 µV		152.6 µV		305.2 µV	
HF path, DC, fixed 50 Ω			<6.9 LSB	<53 µV	<6.9 LSB	<211 µV			<6.9 LSB	<526 µV	<6.9 LSB	<1.05 mV		
Buffered path, full bandwidth	<11 LSB	<67 µV	<7.8 LSB	<119 µV	<7.1 LSB	<217 µV	<12 LSB	<732 µV			<8.1 LSB	<1.24 mV	<7.1 LSB	<2.17 mV
Buffered path, BW limit active	<7.9 LSB	<48 µV	<7.0 LSB	<107 µV	<6.9 LSB	<211 µV	<9.8 LSB	<598 µV			<7.2 LSB	<1.10 mV	<7.1 LSB	<2.17 mV

M4i.441x, M4x.441x, DN2.441-xx and DN6.441-xx, 16 Bit 130 MS/s

Input Range	±200 mV		±500 mV		±1		±2 V		±2.5 V		±5 V		±10 V	
Voltage resolution (1)	6.1 µV		15.3 µV		30.5 µV		61.0 µV		76.3 µV		152.6 µV		305.2 µV	
HF path, DC, fixed 50 Ω			<5.9 LSB	<90 µV	<5.9 LSB	<180 µV			<5.9 LSB	<450 µV	<5.9 LSB	<900 µV		
Buffered path, full bandwidth	<8.5 LSB	<52 µV	<6.5 LSB	<99 µV	<5.9 LSB	<180 µV	<11 LSB	<671 µV			<7.0 LSB	<1.07 mV	<6.1 LSB	<1.86 mV
Buffered path, BW limit active	<7.0 LSB	<43 µV	<6.1 LSB	<93 µV	<5.9 LSB	<180 µV	<9.6 LSB	<586 µV			<6.7 LSB	<1.02 mV	<6.1 LSB	<1.86 mV

Dynamic Parameters

M4i.445x, M4x.445x, DN2.445-xx and DN6.445-xx, 14 Bit 500 MS/s
M4i.448x, M4x.448x, DN2.448-xxx and DN6.448-xx, 14 Bit 400 MS/s

Input Path	HF path, AC coupled, fixed 50 Ohm						Buffered path, BW limit			Buffered path, full BW		
Test signal frequency	10 MHz				40 MHz	70 MHz	10 MHz			10 MHz	40 MHz	70 MHz
Input Range	±500mV	±1V	±2.5V	±5V	±1V	±1V	±200mV	±500mV	±1V	±500mV	±500mV	±500mV
THD (typ) (dB	<-75.9 dB	<-75.8 dB	<-75.2 dB	<-74.8 dB	<-72.5 dB	<-67.4 dB	<-71.4 dB	<-72.1 dB	<-68.6 dB	<-65.0 dB	<-58.6 dB	<-54.4 dB
SNR (typ) (dB)	>67.8 dB	>67.9 dB	>68.0 dB	>68.0 dB	>69.5 dB	>67.5 dB	>67.5 dB	>68.0 dB	>68.1 dB	>67.3 dB	>65.8 dB	>65.6 dB
SFDR (typ), excl. harm. (dB)	>88.1 dB	>88.6 dB	>85.2 dB	>85.3 dB	>88.0 dB	>87.8 dB	>87.3 dB	>88.4 dB	>87.5 dB	>89.0 dB	>88.9 dB	>88.8 dB
SFDR (typ), incl. harm. (dB)	>80.1 dB	>80.0 dB	>77.4 dB	>77.3 dB	>74.0 dB	>69.9 dB	>78.1 dB	>73.5 dB	>69.8 dB	>67.5 dB	>60.8 dB	>56.0 dB
SINAD/THD+N (typ) (dB)	>67.2 dB	>67.2 dB	>67.2 dB	>67.2 dB	>67.7 dB	>64.4 dB	>66.5 dB	>66.6 dB	>65.3 dB	>63.9 dB	>57.9 dB	>54.0 dB
ENOB based on SINAD (bit)	>10.9 bit	>10.9 bit	>10.9 bit	>10.9 bit	>10.9 bit	>10.4 bit	>10.7 bit	>10.8 bit	>10.6 bit	>10.3 bit	>9.3 bit	>8.7 bit
ENOB based on SNR (bit)	>11.0 bit	>11.0 bit	>11.0 bit	>11.0 bit	>11.0 bit	>10.9 bit	>10.9 bit	>11.0 bit	>11.0 bit	>10.9 bit	>10.6 bit	>10.6 bit

M4i.442x, M4x.442x, DN2.442-xx and DN6.442-xx, 16 Bit 250 MS/s
M4i.447x, M4x.447x, DN2.447-xx and DN6.447-xx, 16 Bit 180 MS/s

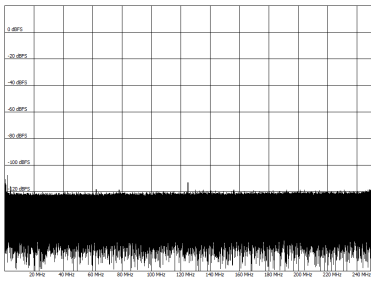
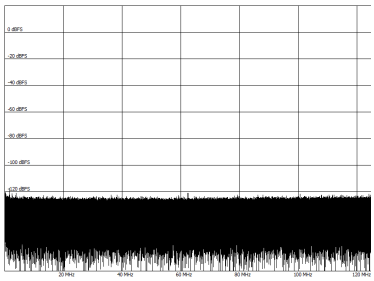
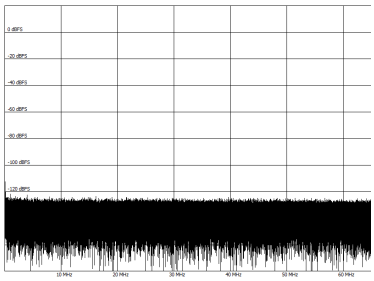
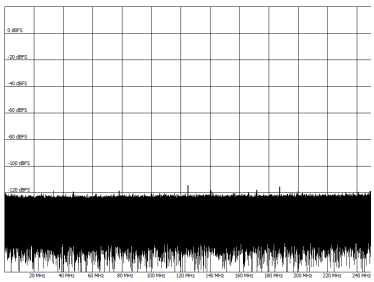
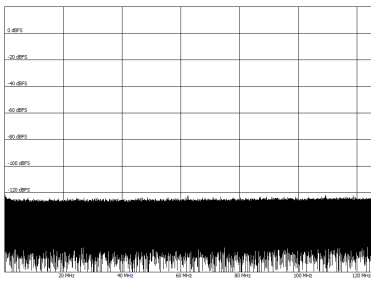
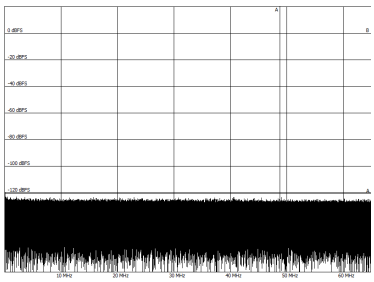
Input Path	HF path, AC coupled, fixed 50 Ohm						Buffered path, BW limit			Buffered path, full BW		
Test signal frequency	1 MHz	10 MHz				40 MHz	10 MHz			1 MHz	10 MHz	40 MHz
Input Range	±1V	±500mV	±1V	±2.5V	±5V	±1V	±200mV	±500mV	±1V	±500mV	±500mV	±500mV
THD (typ) (dB	<-73.1 dB	<-74.0 dB	<-74.1 dB	<-74.1 dB	<-74.1 dB	<-62.9 dB	<-73.2 dB	<-71.5 dB	<-69.0 dB	<-72.2 dB	<-67.5 dB	<49.8 dB
SNR (typ) (dB)	>71.9 dB	>71.5 dB	>71.5 dB	>71.6 dB	>71.6 dB	>71.8 dB	>69.8 dB	>71.0 dB	>71.2 dB	>71.7 dB	>71.0 dB	>69.0 dB
SFDR (typ), excl. harm. (dB)	>92.1 dB	>90.4 dB	>90.8 dB	>90.1 dB	>89.7 dB	>90.2 dB	>92.1 dB	>92.0 dB	>92.1 dB	>90.0 dB	>91.4 dB	>92.5 dB
SFDR (typ), incl. harm. (dB)	>74.4 dB	>75.4 dB	>75.5 dB	>75.5 dB	>75.5 dB	>64.5 dB	>75.0 dB	>73.1 dB	>69.8 dB	>74.7 dB	>67.8 dB	>50.0 dB
SINAD/THD+N (typ) (dB)	>69.8 dB	>69.6 dB	>69.6 dB	>69.6 dB	>69.6 dB	>62.2 dB	>68.5 dB	>68.2 dB	>67.0 dB	>68.8 dB	>66.4 dB	>48.9 dB
ENOB based on SINAD (bit)	>11.3 bit	>11.2 bit	>11.2 bit	>11.3 bit	>11.3 bit	>10.0 bit	>11.1 bit	>11.0 bit	>10.8 bit	>11.1 dB	>10.7 bit	>7.8 bit
ENOB based on SNR (bit)	>11.7 bit	>11.6 bit	>11.6 bit	>11.6 bit	>11.6 bit	>11.6 dB	>11.3 bit	>11.5 bit	>11.5 bit	>11.6 dB	>11.5 bit	>11.2 bit

M4i.441x, M4x.441x, DN2.441-xx and DN6.441-xx, 16 Bit 130 MS/s

Input Path	HF path, AC coupled, fixed 50 Ohm						Buffered path, BW limit			Buffered path, full BW		
Test signal frequency	1 MHz	10 MHz					10 MHz			1 MHz	10 MHz	
Input Range	±1V	±500mV	±1V	±2.5V	±5V		±200mV	±500mV	±1V	±500mV	±500mV	
THD (typ) (dB	<-72.6 dB	<-77.8 dB	<-77.5 dB	<-77.3 dB	<-77.1 dB		<-74.5 dB	<-73.9 dB	<-70.1 dB	<-73.5 dB	<73.4 dB	
SNR (typ) (dB)	>72.2 dB	>71.8 dB	>71.9 dB	>72.0 dB	>72.0 dB		>69.8 dB	>71.2 dB	>71.3 dB	>71.1 dB	>71.0 dB	
SFDR (typ), excl. harm. (dB)	>92.4 dB	>97.0 dB	>96.0 dB	>95.2 dB	>94.8 dB		>89.0 dB	>94.0 dB	>94.5 dB	>88.8 dB	>93.5 dB	
SFDR (typ), incl. harm. (dB)	>73.7 dB	>78.6 dB	>78.2 dB	>75.2 dB	>75.1 dB		>77.6 dB	>77.8 dB	>71.5 dB	>74.7 dB	>73.1 dB	
SINAD/THD+N (typ) (dB)	>69.4 dB	>70.8 dB	>70.8 dB	>70.9 dB	>70.8 dB		>69.0 dB	>69.7 dB	>68.2 dB	>69.2 dB	>69.2 dB	
ENOB based on SINAD (bit)	>11.2 bit	>11.5 bit	>11.5 bit	>11.5 bit	>11.5 bit		>11.2 bit	>11.3 bit	>11.0 bit	>11.2 bit	>11.2 bit	
ENOB based on SNR (bit)	>11.7 bit	>11.6 bit	>11.6 bit	>11.6 bit	>11.6 bit		>11.3 bit	>11.5 bit	>11.5 bit	>11.6 bit	>11.6 bit	

Dynamic parameters are measured at ±1 V input range (if no other range is stated) and 50Ω termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave generated by a signal generator and a matching bandpass filter. Amplitude is >99% of FSR. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits.

Noise Floor Plots (open inputs)

	M4i.445x, M4x.445x, DN2.445-xx, DN6.445-xx Sampling Rate 500 MS/s	**M4i.442x, M4x.442x, DN2.442-xx and DN6.442-xx** Sampling Rate 250 MS/s	**M4i.441x, M4x.441x, DN2.441-xx and DN6.441-xx** Sampling Rate 130 MS/s
Buffered Path 1 MΩ, AC ±1 V range			
HF Path 50 Ω, AC ±500 mV			

Connectors

Analog Inputs/Analog Outputs	SMA female (one for each single-ended input)	Cable-Type: Cab-3mA-xx-xx
Trigger 0 Input	SMA female	Cable-Type: Cab-3mA-xx-xx
Clock Input	SMA female	Cable-Type: Cab-3mA-xx-xx
Trigger 1 Input	SMA female	Cable-Type: Cab-3mA-xx-xx
Clock Output	SMA female	Cable-Type: Cab-3mA-xx-xx
Multi Purpose I/O	MMCX female (3 lines)	Cable-Type: Cab-1m-xx-xx

Environmental and Physical Details

Dimension (Single Card)	(PCB only)	160 mm x 100 mm (Standard 3U)
Width		2 slots
Weight (M4x.44xx series)	maximum	340 g
Weight (M4x.22xx, M4x.66xx series)	maximum	450 g
Warm up time		10 minutes
Operating temperature		0°C to 50°C
Storage temperature		-10°C to 70°C
Humidity		10% to 90%
Dimension of packing	1 or 2 cards	470 mm x 250 mm x 130 cm
Volume weight of packing	1 or 2 cards	4 kgs

PXI Express specific details

PXIe slot type	4 Lanes, PCIe Gen 2 (x4 Gen2)
PXIe hybrid slot compatibility	Fully compatible
Sustained streaming mode (Card-to-System: M4x.22xx, M4x.44xx)	> 1.7 GB/s (measured with a chipset supporting a TLP size of 256 bytes, using PXIe x4 Gen2)
Sustained streaming mode (System-to-Card: M4x.66xx)	> 1.4 GB/s (measured with a chipset supporting a TLP size of 256 bytes, using PXIe x4 Gen2)

Certification, Compliance, Warranty

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark
Product warranty	5 years starting with the day of delivery
Software and firmware updates	Life-time, free of charge

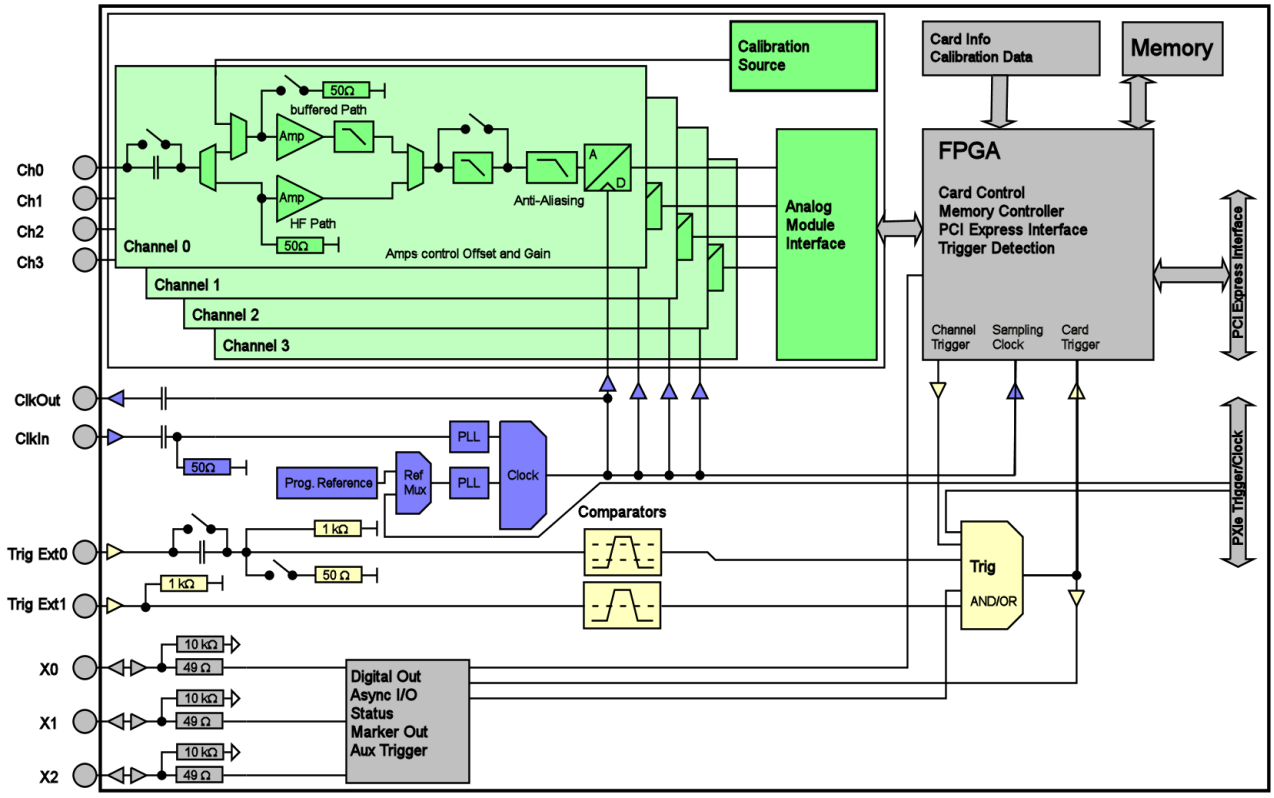
Power Consumption

	PXI EXPRESS		
	3.3V	12 V	Total
M4x.4410-x4, M4x.4420-x4, M4x.4470-x4	0.25 A	2.2 A	27 W
M4x.4411-x4, M4x.4421-x4, M4x.4471-x4	0.25 A	2.7 A	33 W
M4x.4450-x4, M4x.4480-x4	0.25 A	2.2 A	28 W
M4x.4451-x4, M4x.4481-x4	0.25 A	2.9 A	35 W

MTBF

MTBF	200000 hours

Hardware block diagram



Order Information

The card is delivered with 2 GSample on-board memory and supports standard acquisition (Scope), FIFO acquisition (streaming), Multiple Recording, Gated Sampling, Boxcar Average (High-Resolution), ABA mode and Timestamps. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows and Linux), IVI, .NET, Delphi, Java, Python and a Base license of the oscilloscope software SBench 6 are included.

Adapter cables are not included. Please order separately!

PXI Express x4

	Order no.	A/D Resolution	Standard mem	1 channel	2 channels	4 channels
	M4x.4410-x4	16 Bit	2 GSample	130 MS/s	130 MS/s	
	M4x.4411-x4	16 Bit	2 GSample	130 MS/s	130 MS/s	130 MS/s
	M4x.4420-x4	16 Bit	2 GSample	250 MS/s	250 MS/s	
	M4x.4421-x4	16 Bit	2 GSample	250 MS/s	250 MS/s	250 MS/s
	M4x.4450-x4	14 Bit	2 GSample	500 MS/s	500 MS/s	
	M4x.4451-x4	14 Bit	2 GSample	500 MS/s	500 MS/s	500 MS/s
Export Versions	M4x.4470-x4	16 Bit	2 GSample	180 MS/s	180 MS/s	
	M4x.4471-x4	16 Bit	2 GSample	180 MS/s	180 MS/s	180 MS/s
	M4x.4480-x4	14 Bit	2 GSample	400 MS/s	400 MS/s	
	M4x.4481-x4	14 Bit	2 GSample	400 MS/s	400 MS/s	400 MS/s

Firmware Options

Order no.	Option
M4i.xxxx–spavg	Signal Processing Firmware Option: Block Average (later firmware - upgrade available)
M4i.xxxx-spstat	Signal Processing Firmware Option: Block Statistics/Peak Detect (later firmware - upgrade available)

Services

Order no.	
Recal	Recalibration at Spectrum incl. calibration protocol

Standard Cables

		Order no.				
for Connections	Length	to BNC male	to BNC female	to SMA male	to SMA female	to SMB female
Analog/Clock-In/Clk-Out/Trig-In	80 cm	Cab-3mA-9m-80	Cab-3mA-9f-80	Cab-3mA-3mA-80		Cab-3f-3mA-80
	200 cm	Cab-3mA-9m-200	Cab-3mA-9f-200	Cab-3mA-3mA-200		Cab-3f-3mA-200
Trig-Out/Extra	80 cm	Cab-1m-9m-80	Cab-1m-9f-80	Cab-1m-3mA-80	Cab-1m-3fA-80	Cab-1m-3f-80
	200 cm	Cab-1m-9m-200	Cab-1m-9f200	Cab-1m-3mA-200	Cab-1m-3fA-200	Cab-1m-3f-200
Information	The standard adapter cables are based on RG174 cables and have a nominal attenuation of 0.3 dB/m at 100 MHz and 0.5 dB/m at 250 MHz. For high speed signals we recommend the low loss cables series CHF					

Low Loss Cables

Order No.	Option
CHF-3mA-3mA-200	Low loss cables SMA male to SMA male 200 cm
CHF-3mA-9m-200	Low loss cables SMA male to BNC male 200 cm
Information	The low loss adapter cables are based on MF141 cables and have an attenuation of 0.3 dB/m at 500 MHz and 0.5 dB/m at 1.5 GHz. They are recommended for signal frequencies of 200 MHz and above.

Amplifiers

Order no.	Bandwidth	Connection	Input Impedance	Coupling	Amplification
SPA.1412 [2]	200 MHz	BNC	1 MOhm	AC/DC	x10/x100 (20/40 dB)
SPA.1411 [2]	200 MHz	BNC	50 Ohm	AC/DC	x10/x100 (20/40 dB)
SPA.1232 [2]	10 MHz	BNC	1 MOhm	AC/DC	x100/x1000 (40/60 dB)
SPA.1231 [2]	10 MHz	BNC	50 Ohm	AC/DC	x100/x1000 (40/60 dB)
Information	External Amplifiers with one channel, BNC/SMA female connections on input and output, manually adjustable offset, manually switchable settings. An external power supply for 100 to 240 VAC is included. Please be sure to order an adapter cable matching the amplifier connector type and matching the connector type for your A/D card input.				

Software SBench6

Order no.	
SBench6	Base version included in delivery. Supports standard mode for one card.
SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
Volume Licenses	Please ask Spectrum for details.

Software Options

Order no.	
SPc-RServer	Remote Server Software Package - LAN remote access for M2i/M3i/M4i/M4x/M2p cards
SPc-SCAPP	Spectrum's CUDA Access for Parallel Processing - SDK for direct data transfer between Spectrum card and CUDA GPU. Includes RDMA activation and examples.

[1] : Just one of the options can be installed on a card at a time.
[2] : Third party product with warranty differing from our export conditions. No volume rebate possible.

Technical changes and printing errors possible