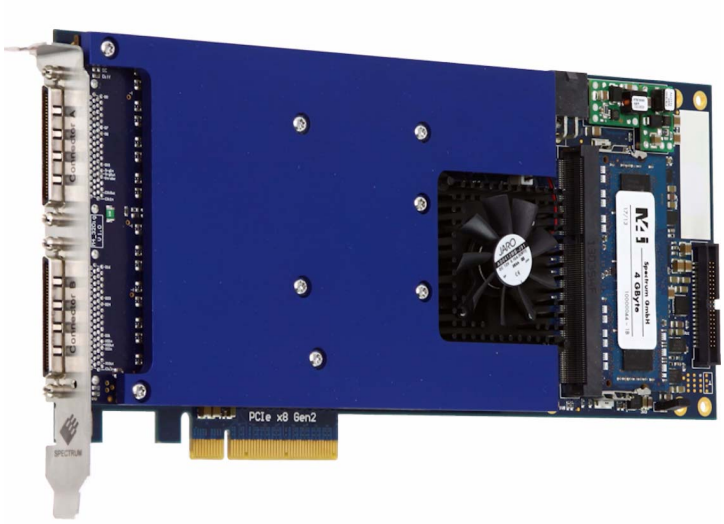
M4i.77xx-x8 - 32 Channel Digital Waveform Acquisition

- **Up to 720 MBit/s sampling rate in timing analysis mode**
- **Up to 700 MBit/s DDR sampling rate in state clock mode (clock gaps allowed)**
- **Differential interface version (for LVDS, (LV)PECL, (N)ECL and other differential signals)**
- **Programmable clock delay**
- **Single-ended interface version for logic levels 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V**
- **Ultra Fast PCI Express x8 Gen 2 interface**
- **4 GByte on-board memory (up to 1 GBit per channel)**
- **FIFO mode continuous streaming**
- **Modes: Single-Shot, Multiple Recording, Gated Sampling, Timestamp**
- **Trigger input/output with AND/OR functionality**
- **Synchronization of up to 8 cards per system**

- PCIe x8 Gen 2 Interface
- Works with x8/x16* PCIe slots
- Sustained streaming mode more than 3.4 GB/s**



Operating Systems	Recommended Software	Drivers
• Windows 7 (SP1), 8, 10, Server 2008 R2 and newer • Linux Kernel 2.6, 3.x, 4.x, 5.x • Windows/Linux 32 and 64 bit	• Visual C++, Delphi, C++ Builder, GNU C++, VB.NET, C#, J#, Java, Python • SBench 6	• MATLAB • LabVIEW

Model	Interface	Channels	Sampling Clock	State Clock
M4i.7710-x8	Single-Ended	32	125 MBit/s	125 MBit/s
M4i.7720-x8	Single-Ended	32	250 MBit/s	250 MBit/s
M4i.7730-x8	Single-Ended	32	720 MBit/s	700 MBit/s
M4i.7725-x8	differential	32	250 MBit/s	250 MBit/s
M4i.7735-x8	differential	32	720 MBit/s	700 MBit/s

General Information

The M4i.77xx-x8 series digital waveform acquisition (logic-analyzer) cards include versions with 32 synchronous channels, either single-ended with programmable threshold levels or differential. The large on-board memory can be segmented to record different waveform sequences.

The cards feature a PCI Express x8 Gen 2 interface that offers outstanding data streaming performance. The interface and Spectrum's optimized drivers enable data transfer rates in excess of 3.4 GByte/s** (24 GBit/s) so that all channels can continuously be recorded, even at full sample rate.

While the M4i.77xx cards have been designed using the latest technology they are still software compatible with the drivers from earlier Spectrum digital acquisition cards. Therefore existing customers can use the same software they developed for a 10 year old 60 MS/s digital input card also for an M4i.77xx series 720 MS/s logic analyzer.

*Some x16 PCIe slots are for the use of graphic cards only and can't be used for other cards. **Throughput measured with a motherboard chipset supporting a TLP size of 256 bytes.

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Software Support

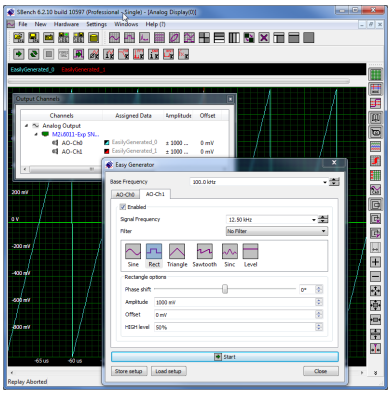
Windows drivers

The cards are delivered with drivers for Windows 7, Windows 8 and Windows 10 (32 bit and 64 bit). Programming examples for Visual C++, C++ Builder, Delphi, Visual Basic, VB.NET, C#, J#, Python, Java and IVI are included.

Linux Drivers

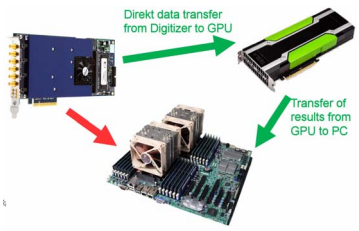
All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like Fedora, Suse, Ubuntu LTS or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for GNU C++, Python as well as the possibility to get the driver sources for your own compilation.

SBench 6



A base license of SBench 6, the easy-to-use graphical operating software for Spectrum cards, is included in the delivery. The base license makes it is possible to test the card, generate simple signals or load and replay previously stored SBench 6 signals. It's a valuable tool for checking the cards performance and assisting with the units initial setup. The cards also come with a demo license for the SBench6 professional version. This license gives the user the opportunity to test the additional features of the professional version with their hardware. The professional version contains several advanced measurement functions, such as FFTs and X/Y display, import and export utilities as well as support for all replay modes including data streaming. Data streaming allows the cards to continuously replay data and transfer it directly from the PC RAM or hard disk. SBench 6 has been optimized to handle data files of several GBytes. SBench 6 runs under Windows as well as Linux (KDE and GNOME) operating systems. A test version of SBench 6 can be downloaded directly over the internet and can run the professional version in a simulation mode without any hardware installed. Existing customers can also request a demo license for the professional version from Spectrum. More details on SBench 6 can be found in the SBench 6 data sheet.

SCAPP – CUDA GPU based data processing



For applications requiring high performance signal and data processing Spectrum offers SCAPP (Spectrum's CUDA Access for Parallel Processing). The SCAPP SDK allows a direct link between Spectrum digitizers, AWGs or Digital Data Acquisition Cards and CUDA based GPU cards. Once in the GPU users can harness the processing power of the GPU's multiple (up to 5000) processing cores and large (up to 24 GB) memories. SCAPP uses an RDMA (Linux only) process to send data at the full PCIe transfer speed to and from the GPU card. The SDK includes a set of examples for interaction between the Spectrum card and the GPU card and another set of CUDA parallel processing examples with easy building blocks for basic functions like filtering, averaging, data demultiplexing, data conversion or FFT. All the software is based on C/C++ and can easily be implemented, expanded and modified with normal programming skills.

Third-party products

Spectrum supports the most popular third-party software products such as LabVIEW, MATLAB or LabWindows/CVI. All drivers come with detailed documentation and working examples are included in the delivery. Support for other software packages, like VEE or DasyLab, can also be provided on request.

Hardware features and options

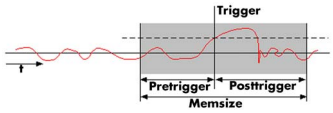
PCI Express x8

The M4i series cards use a PCI Express x8 Gen 2 connection. They can be used in PCI Express x8 and x16 slots with Gen 1, Gen 2, Gen 3 or Gen4. The maximum sustained data transfer rate is more than 3.3 GByte/s (read direction) or 2.8 GByte/s (write direction) per slot. Server motherboards often recognize PCI Express x1, x2 or x4 connections in x8 or x16 slots. These slots can also be used with the M4i series cards but with reduced data transfer rates.

Connections

- The cards are equipped with two VHDCI connectors for the digital channels as well as for the external trigger, clock input and clock output. These connectors also provide two seperate multi-function inputs as well as multi-function outputs that can be individually programmed to perform different functions:
- Trigger output
- Status output (armed, triggered, ready, ...)
- Asynchronous I/O lines

Ring buffer mode

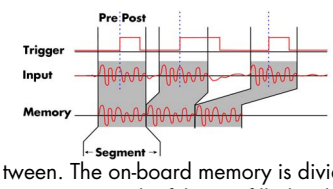


The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

FIFO mode

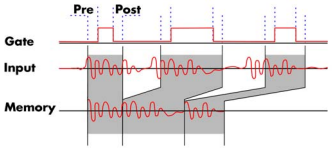
The FIFO or streaming mode is designed for continuous data transfer between the digitizer card and the PC memory. When mounted in a PCI Express x8 Gen 2 interface read streaming speeds of up to 3.4 GByte/s are possible. The control of the data stream is done automatically by the driver on interrupt request basis. The complete installed onboard memory is used to buffer the data, making the continuous streaming process extremely reliable.

Multiple Recording



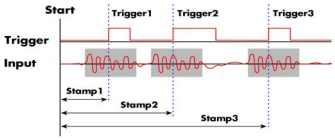
The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

Gated Sampling



The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp



The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronized to a radio clock, an IRIG-B a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

Pattern trigger

Pattern triggers can be defined for every bit of the digital input data. Each input for the pattern trigger can be set to high or low, depending on the expected level, or "don't care". In addition, edge detection can be used to allow triggering on rising , falling or both edges. The pattern trigger can be used to recognize a huge variety of trigger events.

External trigger input

The boards can be triggered using an external trigger input, that has the same exact interface capabilities as the installed data lines, either single-ended with programmable threshold or differential.

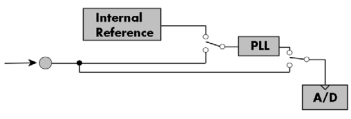
External clock input and output

Using a dedicated input line, that has the same exact interface capabilities as the installed data lines (either single-ended with programmable threshold or differential) a sampling clock can be fed in from an external system. Additionally it's also possible to output the internally used sampling clock on a separate line to synchronize external equipment to this clock.

State clock

The state analysis mode allows to use an external clock to synchronously sample the applied data. In this mode the clock is allowed to have gaps, as long as the minimum required high and low times are met. To simplify the synchronous sampling of the data, the incoming clock signal can be shifted/delayed with regards to the data, to allow proper data capture.

Reference clock



The option to use a precise external reference clock (typically 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the stability of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Star-Hub

The Star-Hub is an additional module allowing the phase stable synchronization of up to 8 boards of a kind in one system. Independent of the number of boards there is no phase delay between all channels. The Star-Hub distributes trigger and clock information between all boards to ensure all connected boards are running with the same clock and trigger. All trigger sources can be combined with a logical OR allowing all channels of all cards to be the trigger source at the same time.

Technical Data

Differential Interface

Available inputs		Data D0 to D31, Trigger (TrigIn), Strobe, Clock (ClkIn), X0, X1
Data Channel Selection	software programmable	32 channels, 16 channels, 8 channels
Data/Control Input Compatibility		LVDS, LVPECL, PECL, (N)ECL, universal differential inputs
Input Coupling		DC
Input Type		high-speed comparator
Input maximum voltage levels		-3.0 V to +5.0 V, max difference between inputs ±8 V
Input voltage hysteresis		25 mV
Input termination		differential termination with 125 Ω
Open inputs		fail save -> defined and fixed input level with open inputs, no external termination necessary
Available outputs		Clock (ClkOut), Trigger (TrigOut), X0, X1
Output signal type		LVDS

Single-Ended Interface

Available inputs		Data D0..D31, Trigger (TrigIn), Strobe, Clock (ClkIn), Multi-Purpose In (X0,X1) + Out (X0,X1,X2)
Data Channel Selection	software programmable	32 channels, 16 channels, 8 channels
Data/Control Input Compatibility		compatible to 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V (LV)TTL and (LV)CMOS logic levels
Input Coupling		DC
Input Type		high-speed comparator
Input threshold level	software programmable	0.0 V up to 4.0 V in steps of 10 mV, separately programmable for (D0..D7), (D8..D15), (D16..D23), (D24..D31), TrigIn, ClkIn, StrobeIn, (X0..X1)
Input maximum voltage levels		-3.0 V to +5.0 V
Input voltage hysteresis		25 mV
Input termination	software programmable	75 Ω (to GND) / 4.7 kΩ (to GND) separately programmable for (D0..D7), (D8..D15), (D16..D23), (D24..D31), TrigIn, ClkIn, StrobeIn, X0, X1
Open inputs		fail save -> defined and fixed input level with open inputs, no external termination necessary
Available outputs		Clock (ClkOut), Multi-Purpose Out (X0, X1, X2)
Output signal type		3.3V LVTTL compatible

Trigger

Available trigger sources	software programmable	External trigger, pattern trigger, software
Trigger edge	software programmable	Rising edge, falling edge or both edges
Trigger delay	software programmable	0 to (8GSamples - 32) = 8589934576 Samples in steps of 32 samples
Multi, Gate: re-arming time		40 samples (+ programmed pretrigger)
Pretrigger at Multi, Gate, FIFO	software programmable	32 up to 4096 samples in steps of 32
Posttrigger	software programmable	32 up to 8G samples in steps of 32 (defining pretrigger in standard scope mode)
Memory depth	software programmable	32 up to [installed memory / number of active channels] samples in steps of 32
Multiple Recording segment size	software programmable	32 up to [installed memory / 2 / active channels] samples in steps of 32
Internal/External trigger accuracy		1 sample
Timestamp modes	software programmable	Standard, Startreset, external reference clock on X1 (e.g. PPS from GPS, IRIG-B)
Data format		Std., Startreset: 64 bit counter, increments with sample clock (reset manually or on start) RefClock: 24 bit upper counter (increment with RefClock) 40 bit lower counter (increments with sample clock, reset with RefClock)
Extra data	software programmable	none, acquisition of X0/X1 inputs at trigger time
Size per stamp		128 bit = 16 bytes

Multi Purpose I/O lines (on VHDCI connector)

Number of multi purpose lines		three named X0 and X1, separate lines for input and output, X2 (output only)
Input: available signal types	software programmable	Asynchronous Digital-In, Timestamp Reference Clock
Output: available signal types	software programmable	Asynchronous Digital-Out, Run, Arm, Trigger, PLL RefClk
Multi Purpose input impedance (Diff.)		differential termination with 125 Ω
Multi Purpose input impedance (SE)	software programmable	75 Ω (to GND) / 4.7 kΩ (to GND), separately programmable for X0 and X1
Multi Purpose input type (Diff.)		LVDS, LVPECL, PECL, (N)ECL, universal differential inputs
Multi Purpose input type (SE)		compatible to 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V (LV)TTL and (LV)CMOS logic levels
Multi Purpose input threshold level (SE)	software programmable	0.0 V up to 4.0 V in steps of 10 mV (common programmable level for X0 and X1)
Multi Purpose output type (Diff.)		Differential LVDS
Multi Purpose output type (SE)		3.3V LVTTL compatible

Power Source (on VHDCI connector)

Number of power pins	6
Voltage	3.3 V
Maximum current	500 mA combined on all pins
Fuse	Self resetting fuse (PTC)

Clock

Clock Modes	software programmable	internal PLL, external reference clock, state clock, sync
Internal clock accuracy		≤ ±20 ppm
Internal clock setup granularity		1 Hz
Clock setup range gaps		562 MHz to 574 MHz (no clock setup possible in that range)
Primary Clk-In (Ext0) as reference clock		
External reference clock range	software programmable	≥ 10 MHz and ≤ 1 GHz
External reference clock input impedance (Diff.)		differential termination with 125 Ω
External reference clock input type (Diff.)		LVDS, LVPECL, PECL, (N)ECL, universal differential inputs
External reference clock input type (SE)		compatible to 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V (LV)TTL and (LV)CMOS logic levels
External reference clock input impedance (SE)	software programmable	75 Ω (to GND) / 4.7 kΩ (to GND)
External reference clock input threshold level (SE)	software programmable	0.0 V up to 4.0 V in steps of 10 mV
External reference clock input edge		Rising edge
External reference clock input duty cycle requirement		45% to 55%
External reference clock input requirements		no frequency changes, no gaps
Primary Clk-In (Ext0) as state clock		
External state clock input coupling		DC
External state clock input impedance (Diff.)		differential termination with 125 Ω
External state clock input impedance (SE)	software programmable	75 Ω (to GND) / 4.7 kΩ (to GND)
External state clock input type (Diff.)		LVDS, LVPECL, PECL, (N)ECL, universal differential inputs
External state clock input type (SE)		compatible to 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V (LV)TTL and (LV)CMOS logic levels
External state clock input threshold level (SE)	software programmable	0.0 V up to 4.0 V in steps of 10 mV
External state clock input edge	software programmable	Rising edge or falling edge (SDR) or both edges (DDR)
External state clock input requirements		Any frequency within specification, changes allowed, gaps allowed, DC allowed
External state clock delay	software programmable	0 ps to 2000 ps with a step size of 40 ps
Secondary Clk-In-AC (Ext1) as state clock		
External secondary clock input coupling		AC
External secondary clock input impedance		differential termination with 100 Ω
External secondary clock input type		LVPECL
External secondary clock input voltage swing		(ClkIn-AC+ to ClkIn-AC–): ±100 mV up to ±1.7 V
Sampling clock output type (Diff.)		Differential LVDS
Sampling clock output type (SE)		3.3V LVTTL compatible
Sampling clock output frequency	Internal or External reference	½ of internal sampling clock (disabled for frequencies above 125 MHz on SE models)
Sampling clock output frequency	External state clock	Copy of fed in state clock (not available for M4i.7730)
Star-Hub synchronization clock modes	software selectable	Internal clock, External reference clock (state clock is not available with synchronization)

Clock Limits

	M4i.7710-x8	**M4i.7720-x8**	**M4i.7730-x8**	**M4i.7725-x8**	**M4i.7735-x8**
Interface	Single-Ended	Single-Ended	Single-Ended	Differential	Differential
minimum internal clock	610 S/s	610 S/s	610 S/s	610 S/s	610 S/s
maximum internal clock	125 MS/s	250 MS/s	720 MS/s	250 MS/s	720 MS/s
minimum state clock (Ext 0)	DC	DC	DC	DC	DC
minimum state clock (Ext 1)	30 kHz	30 kHz	30 kHz	30 kHz	30 kHz
maximum state clock (single data rate)	125 MHz	250 MHz	350 MHz	250 MHz	350 MHz
maximum state clock (double data rate)	62.5 MHz	125 MHz	350 MHz	125 MHz	350 MHz
maximum state clock data rate (SDR)	125 MBit/s	250 MBit/s	350 MBit/s	250 MBit/s	350 MBit/s
maximum state clock data rate (DDR)	125 MBit/s	250 MBit/s	700 MBit/s	250 MBit/s	700 MBit/s

Timings

		Signal type	**External reference clock Input Ext 0**	**State Clock Input Ext 0**		**State Clock Input Ext 1**	
			No Clk Delay	No Clk Delay	Max. Clk Delay	No Clk Delay	Max. Clk Delay
t_{setup}	Setup time before clock edge	input signals	TBD	720 ps	-1280 ps	TBD	TBD
t_{hold}	Hold time after clock edge	input signals	TBD	200 ps	2200 ps	TBD	TBD
t_{delay}	Delay from clock input to clock output	input signals	TBD	TBD	TBD	TBD	TBD

Connectors

Number of connectors	2
Connector type	68 pin standard VHDCI
Connector impedance	125 Ω (differential), 75 Ω (single-ended),
Cable recommendations	compatible to SCSI ultra-320, double shielded, twisted pair, max length 1 m, cable twisting: Pin1/Pin35, Pin2/Pin36 ... Pin 34/68

Environmental and Physical Details

Dimension (Single Card)		L x H x W: 241 mm (¾ PCIe length) x 107 mm x 20 mm (single slot width)
Dimension (Card with option SH8tm installed)		241 mm (¾ PCIe length) x 107 mm x 40 mm (double slot width, extends W by 1 slot right of the main card's bracket, on „component side" of the PCIe card.)
Dimension (Card with option SH8ex installed)		Extends L to 312 mm (full PCIe length) x 107 mm x 20 mm (single slot width)
Dimension (Card with option M4i.44xx-DigSMA installed)		241 mm (¾ PCIe length) x 107 mm x 40 mm (double slot width, extends W by 1 slot left of the main card's bracket, on „solder side" of the PCIe card.)
Weight (M4i.44xx series)	maximum	290 g
Weight (M4i.22xx, M4i.23xx, M4i.66xx, M4i.77xx series)	maximum	420 g
Weight (Option star-hub -sh8ex, -sh8tm)	including 8 sync cables	130 g
Weight (Option M4i.44xx-DigSMA)		TBD g
Warm up time		10 minutes
Operating temperature		0°C to 50°C
Storage temperature		-10°C to 70°C
Humidity		10% to 90%
Dimension of packing	1 or 2 cards	470 mm x 250 mm x 130 cm
Volume weight of packing	1 or 2 cards	4 kgs

PCI Express specific details

PCIe slot type	x8 Generation 2
PCIe slot compatibility (physical)	x8/x16
PCIe slot compatibility (electrical)	x1, x2, x4, x8, x16 with Generation 1, Generation 2, Generation 3, Generation 4
Sustained streaming mode (Card-to-System): M4i.22xx, M4i.23xx, M4i.44xx, M4i.77xx	> 3.4 GB/s (measured with a chipset supporting a TLP size of 256 bytes, using PCIe x8 Gen2)
Sustained streaming mode (System-to-Card): M4i.66xx	> 2.8 GB/s (measured with a chipset supporting a TLP size of 256 bytes, using PCIe x8 Gen2)

Certification, Compliance, Warranty

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark
Product warranty	5 years starting with the day of delivery
Software and firmware updates	Life-time, free of charge

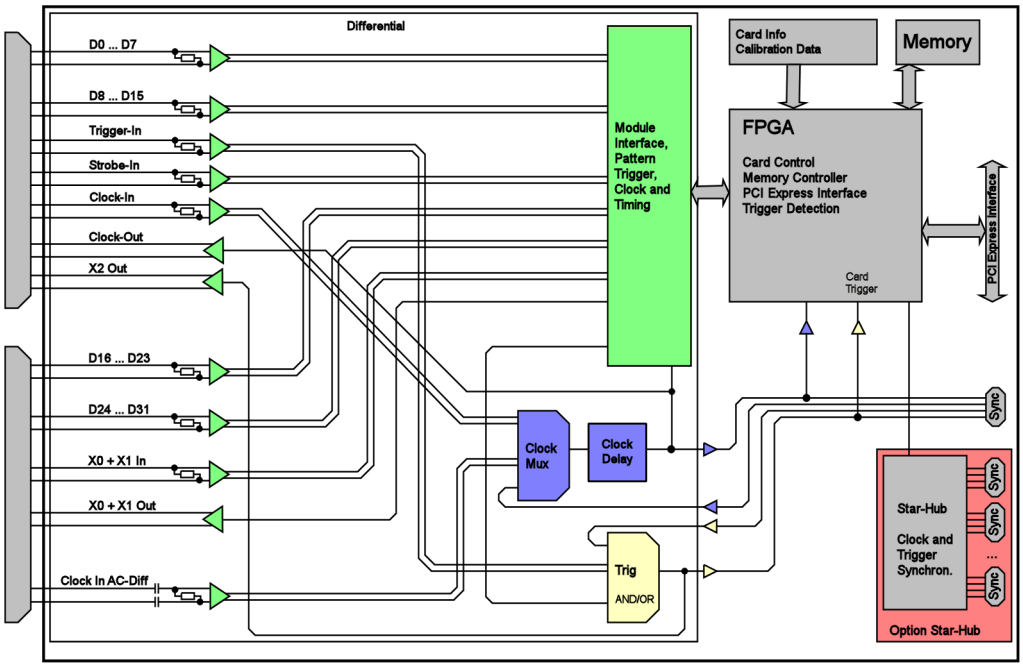
Power Consumption

		PCI EXPRESS		
		3.3V	**12 V**	**Total**
M4i.771x-x8, M4i.772x-x8	Power output 0mA	0.2 A	2.9 A	36 W
M4i.773x-x8	Power output 0mA	0.2 A	3.1 A	38 W

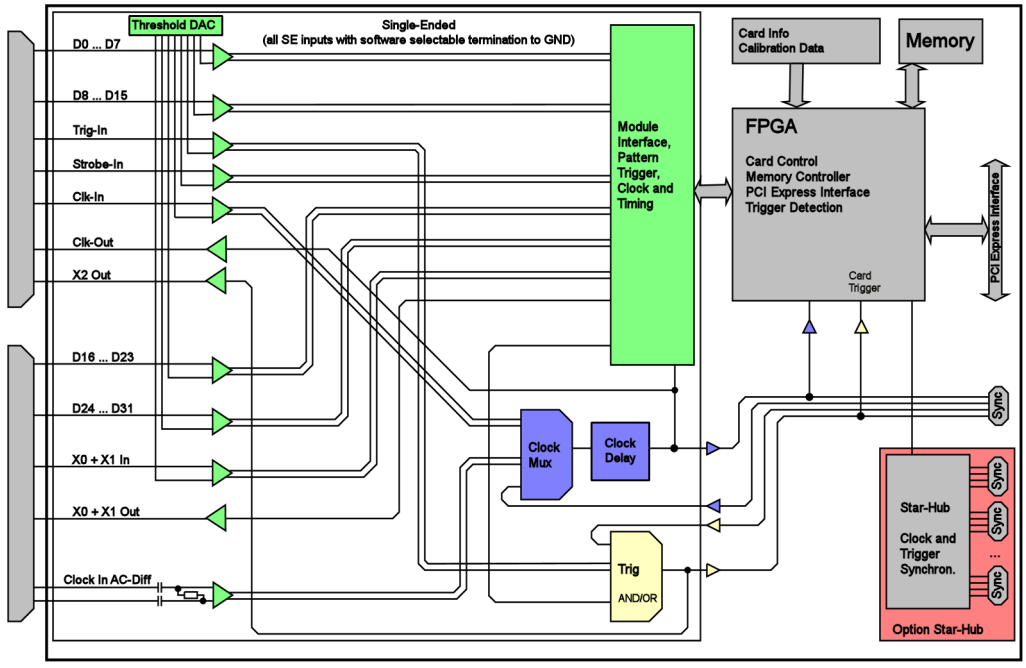
MTBF

MTBF	100000 hours

Block diagram differential input version



Block diagram single-ended input version



Order Information

The card is delivered with 4 GByte on-board memory and supports standard acquisition (Scope), FIFO acquisition (streaming), Multiple Recording, Gated Sampling and Timestamps. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows and Linux), .NET, Delphi, Java, Python and a Base license of the oscilloscope/logic-analyzer software SBench 6 are included.

Adapter cables are not included. Please order separately!

PCI Express x8

Order no.	Channels	Interface	Standard mem	Sampling Clock	State Clock
M4i.7710-x8	32	Single-Ended	4 GByte	125 MBit/s	125 MBit/s
M4i.7720-x8	32	Single-Ended	4 GByte	250 MBit/s	250 MBit/s
M4i.7730-x8	32	Single-Ended	4 GByte	720 MBit/s	700 MBit/s

PCI Express x8

Order no.	Channels	Interface	Standard mem	Sampling Clock	State Clock
M4i.7725-x8	32	Differential	4 GByte	250 MBit/s	250 MBit/s
M4i.7735-x8	32	Differential	4 GByte	720 MBit/s	700 MBit/s

Options

Order no.	Option
M4i.xxxx-SH8ex [1]	Synchronization Star-Hub for up to 8 cards (extension), only one slot width, extension of the card to full PCI Express length (312 mm). 8 synchronization cables included.
M4i.xxxx-SH8tm [1]	Synchronization Star-Hub for up to 8 cards (top mount), two slots width, top mounted on card. 8 synchronization cables included.
M4i-upgrade	Upgrade for M4i.xxxx: Later installation of option Star-Hub

VHDCI Cable

Order no.	Option
Cab-v68-v68-100	Shieleded twisted-pair cable VHDCI to VHDCI, 100 cm, 125 Ω differentiell, 90 Ω single-ended
Cab-v68-v68-300	Shieleded twisted-pair cable VHDCI to VHDCI, 300 cm, 125 Ω differentiell, 90 Ω single-ended

Software SBench6

Order no.	
SBench6	Base version included in delivery. Supports standard mode for one card.
SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
Volume Licenses	Please ask Spectrum for details.

Software Options

Order no.	
SPc-RServer	Remote Server Software Package - LAN remote access for M2i/M3i/M4i/M4x/M2p cards
SPc-SCAPP	Spectrum's CUDA Access for Parallel Processing - SDK for direct data transfer between Spectrum card and CUDA GPU. Includes RDMA activation and examples.

[1] : Just one of the options can be installed on a card at a time.

[2] : Third party product with warranty differing from our export conditions. No volume rebate possible.

Technical changes and printing errors possible