DN2.82x - hybridNETBOX up to 500 MS/s Digitizer and 1.25 GS/s AWG

- **Stimulus-Response, Closed-Loop, Recorder/Replay, Automated Tests, MIMO, ...**
- **2 or 4 channels Digitizer with 180 MS/s up to 500 MS/s**
- **2 or 4 channels AWG with 625 MS/s up to 1.25 GS/s**
- **Simultaneously sampling and generation on all channels**
- **2 GSample acquisition and 2 GSample AWG memory**
- **Digitizer: separate ADC and amplifier per channel**
- **Digitizer: 6 input ranges: ±200 mV up to ±10 V**
- **Digitizer: programmable input offset of ±100%**
- **AWG: output into 50 Ohm up to ±2.5 V (4 channels) or ±2 V (2 channels)**
- **AWG: output into 1 MOhm up to ±5 V (4 channels) or ±4 V (2 channels)**
- **Streaming, Multiple Recording, Gated Sampling, Timestamps, Sequence Replay**

- Ethernet Remote Instrument
- LXI Core 2011 compatible
- GBit Ethernet Interface
- Sustained streaming mode up to 70 MB/s
- Direct Connection to PC/Laptop
- Connect anywhere in company LAN
- Embedded Webserver for Maintenance/Updates
- Embedded Server option for open Linux platform

Operating Systems	**SBench 6 Professional Included**	**Drivers**
• Windows 7 (SP1), 8, 10, Server 2008 R2 and newer • Linux Kernel 2.6, 3.x, 4.x, 5.x • Windows/Linux 32 and 64 bit	• Acquisition, Generation and Display of analog and digital data • Calculation, FFT • Documentation and Import, Export	• LabVIEW, MATLAB, LabWindows/CVI • Visual C++, C++ Builder, GNU C++, VB.NET, C#, Delphi, Java, Python, Julia • IVI

SBench 6 can only operate the cards independently by starting two instances of the program

Model	Digitizer			Arbitrary Waveform Generator			
	Channels	Res.	Sampling Rate	Channels	Res.	Sampling Rate	Output Level
DN2.822-02	2 channels	16 bit	250 MS/s	2 channels	16 bit	1.25 GS/s	±2.0V (50Ω)
DN2.822-04	4 channels	16 bit	250 MS/s	4 channels	16 bit	625 MS/s	±2.5V (50Ω)
DN2.825-02	2 channels	14 bit	500 MS/s	2 channels	16 bit	1.25 GS/s	±2.0V (50Ω)
DN2.825-04	4 channels	14 bit	500 MS/s	4 channels	16 bit	625 MS/s	±2.5V (50Ω)

Export-Versions

Sampling rate limited versions that do not fall under export restrictions.

DN2.827-02	2 channels	16 bit	180 MS/s	2 channels	16 bit	1.25 GS/s	±2.0V (50Ω)
DN2.827-04	4 channels	16 bit	180 MS/s	4 channels	16 bit	625 MS/s	±2.5V (50Ω)
DN2.828-02	2 channels	14 bit	400 MS/s	2 channels	16 bit	1.25 GS/s	±2.0V (50Ω)
DN2.828-04	4 channels	14 bit	400 MS/s	4 channels	16 bit	625 MS/s	±2.5V (50Ω)

General Information

The hybridNETBOX DN2.82x series internally consists of a Digitizer and an AWG that can run together or independently. That allows simultaneous data generation and data acquisition for stimulus-response tests, ATE applications, MIMO applications or closed-loop applications. The hybridNETBOX can be installed anywhere in the company LAN and can be remotely controlled from a host PC.

Synchronization is done externally with the help of clock/trigger-output to clock/trigger-input connection

Software Support

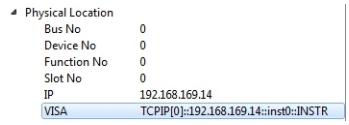
Windows Support

The digitizerNETBOX/generatorNETBOX/hybridNETBOX can be accessed from Windows 7, Windows 8,Windows 10 (either 32 bit or 64 bit). Programming examples for Visual C++, C++ Builder, LabWindows/CVI, Delphi, Visual Basic, VB.NET, C#, Julia, Python, Java and IVI are included.

Linux Support

The digitizerNETBOX/generatorNETBOX/hybridNETBOX can be accessed from any Linux system. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++, Python, Julia as well as drivers for MATLAB for Linux. SBench 6, the powerful data acquisition and analysis software from Spectrum is also included as a Linux version.

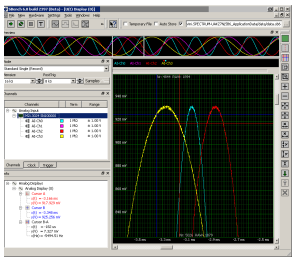
Discovery Protocol



The Discovery function helps you to find and identify any Spectrum LXI instruments, like the digitizerNETBOX and generatorNETBOX, available to your computer on the network. The Discovery function will also locate any Spectrum card products that are managed by an installed Spectrum Remote Server somewhere on the network.

After running the discovery function the card information is cached and can be directly accessed by SBench 6. Furthermore the qualified VISA address is returned and can be used by any software to access the remote instrument.

SBench 6 Professional



The digitizerNETBOX, generatorNETBOX and hybridNETBOX can be used with Spectrum's powerful software SBench 6 – a Professional license for the software is already installed in the box. SBench 6 supports all of the standard features of the instrument. It has a variety of display windows as well as analysis, export and documentation functions.

- Available for Windows Windows 7, Windows 8, Windows 10 and Linux
- Easy to use interface with drag and drop, docking windows and context menus
- Display of analog and digital data, X-Y display, frequency domain and spread signals
- Designed to handle several GBytes of data
- Fast data preview functions
- SBench 6 only supports either AWG or Digitizer in one program
- Star-Hub for mixed mode applications is not supported
- To run AWG and Digitizer with SBench 6, the software needs to be started twice and each instance of the program then operates independetly one device

IVI Driver

The IVI standards define an open driver architecture, a set of instrument classes, and shared software components. Together these provide critical elements needed for instrument interchangeability. IVI's defined Application Programming Interfaces (APIs) standardize common measurement functions reducing the time needed to learn a new IVI instrument.

The Spectrum products to be accessed with the IVI driver can be locally installed data acquisition cards, remotely installed data acquisition cards or remote LXI instruments like digitizerNETBOX/generatorNETBOX. To maximize the compatibility with existing IVI based software installations, the Spectrum IVI driver supports IVI Scope, IVI Digitizer and IVI FGen class with IVI-C and IVI-COM interfaces.

Third-party Software Products

Most popular third-party software products, such as LabVIEW, MATLAB or LabWindows/CVI are supported. All drivers come with examples and detailed documentation.

Embedded Webserver

The integrated webserver follows the LXI standard and gathers information on the product, set up of the Ethernet configuration and current status. It also allows the setting of a configuration password, access to documentation and updating of the complete instrument firmware, including the embedded remote server and the webserver.

General Hardware features and options

LXI Instrument

The digitizerNETBOX and generatorNETBOX are fully LXI instrument compatible to LXI Core 2011 following the LXI Device Specification 2011 rev. 1.4. The digitizerNETBOX/generatorNETBOX has been tested and approved by the LXI Consortium.

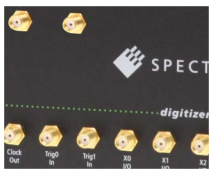
Located on the front panel is the main on/off switch, LEDs showing the LXI and Acquisition status and the LAN reset switch.

Chassis features

The chassis is especially designd for usage in different application arreas and has some advanced features for mobile and shared usage:

- stable metal chassis
- 8 bumper edges protect the chassis, the desk and other components on it. The bumper edges allow to store the chassis either vertically or horizontally and the lock-in structure allows to stack multiple chassis with a secure fit onto each other. For 19" rack mount montage the bumpers can be unmounted and replaced by the 19" rack mount option
- The handle allows to easily carry the chassis around in juts one hand.
- A standard GND screw on the back of the chassis allows to connect the metal chassis to measurement ground to reduce noise based on ground loops and ground level differences.

Front Panel



Standard SMA connectors are used for all analog input signals and all trigger and clock signals. No special adapter cables are needed and the connection is secure even when used in a moving environment.

Custom front panels are available on request even for small series, be it BNC, LEMO connectors or custom specific connectors.

Ethernet Connectivity

The GBit Ethernet connection can be used with standard COTS Ethernet cabling. The integration into a standard LAN allows to connect the digitizerNETBOX/generatorNETBOX either directly to a desktop PC or Laptop or it is possible to place the instrument somewhere in the company LAN and access it from any desktop over the LAN.

Boot on Power Option

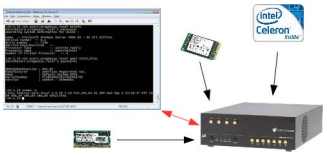
The digitizerNETBOX/generatorNETBOX can be factory configured to automatically start and boot upon availability of the input power rail. That way the instrument will automatically become available again upon loss of input power.

DC Power Supply Option

The digitizerNETBOX/generatorNETBOX can be equipped with an internal DC power supply which replaces the standard AC power supply. Two different power supply options are available that range from 9V to 36V. Contact the sales team if other DC levels are required.

Using the DC power supply the digitizerNETBOX/generatorNETBOX can be used for mobile applications together with a Laptop in automotive or airborne applications.

Option Embedded Server



The option turns the digitizerNETBOX/generatorNETBOX in a powerful PC that allows to run own programs on a small and remote data acquisition system. The digitizerNETBOX/generatorNETBOX is enhanced by more memory, a powerful CPU, a freely accessable internal SSD and a remote software development access method.

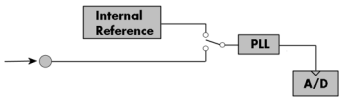
The digitizerNETBOX/generatorNETBOX can either run connected to LAN or it can run totally independent, storing data to the internal SSD. The original digitizerNETBOX/generatorNETBOX remote instrument functionality is still 100 % available. Running the embedded server option it is possible to pre-calculate results based on the acquired data, store acquisitions locally and to transfer just the required data or results parts in a client-server based software structure. A different example for the digitizerNETBOX/generatorNETBOX embedded server is surveillance/logger application which can run totally independent for days and send notification emails only over LAN or offloads stored data as soon as it's connected again.

Access to the embedded server is done through a standard text based Linux shell based on the ssh secure shell.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock



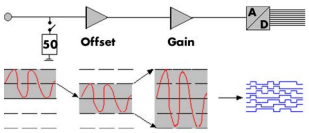
The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Export Versions

Special export versions of the products are available that do not fall under export control. Products fall under export control if their specification exceeds certain sampling rates at a given A/D resolution and if the product is shipped into a country where no general export authorization is in place.

The export versions of the products have a sampling rate limitation matching the export control list. An upgrade to the faster version is not possible. The sampling rate limitation is in place for both internal and external clock.

Digitizer Hardware Features and Options



Software selectable input path

For each of the analog channels the user has the choice between two analog input paths. The „Buffered" path offers the highest flexibility when it comes to input ranges and termination. A software programmable 50 Ohm and 1 MOhm termination also allows to connect standard oscilloscope probes to the card. The „50 Ohm" path on the other hand provides the highest bandwidth and the best signal integrity with a fewer number of input ranges and a fixed 50 Ohm termination.

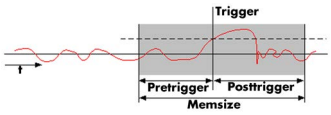
Software selectable lowpass filter

Each analog channel contains a software selectable low-pass filter to limit the input bandwidth. Reducing the analog input bandwidth results in a lower total noise and can be useful especially with low voltage input signals.

Automatic on-board calibration

All of the channels are calibrated in factory before the board is shipped. To compensate for different variations like PC power supply, temperature and aging, the software driver provides routines for an automatic onboard offset and gain calibration of all input ranges. All the cards contain a high precision on-board calibration reference.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

FIFO mode

The FIFO mode is designed for continuous data transfer between remote instrument and PC memory or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

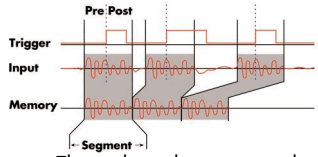
Channel trigger

The data acquisition instruments offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses. In addition to this a re-arming mode (for accurate trigger recognition on noisy signals) the AND/OR conjunction of different trigger events is possible. As a unique feature it is possible to use deactivated channels as trigger sources.

External trigger input

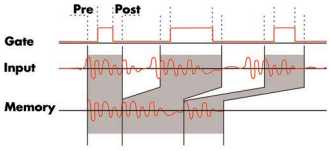
All boards can be triggered using up to two external analog or digital signals. One external trigger input has two analog comparators that can define an edge or window trigger, a hysteresis trigger or a rearm trigger. The other input has one comparator that can be used for standard edge and level triggers.

Multiple Recording



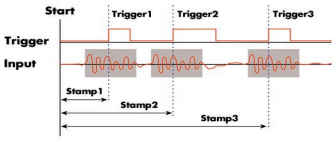
The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

Gated Sampling



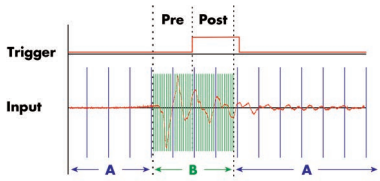
The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp



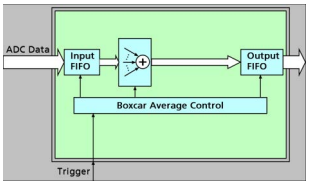
The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronized to a radio clock, an IRIG-B a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

ABA mode



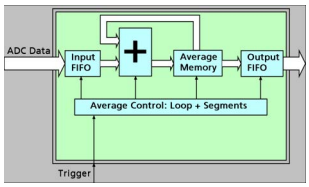
The ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

Boxcar Average (high-resolution) mode



The Boxcar average or high-resolution mode is a form of averaging. The ADC oversamples the signal and averages neighboring points together. This mode uses a real-time boxcar averaging algorithm that helps reducing random noise. It also can yield a higher number of bits of resolution depening on the signal acquired. The averaging factor can be set in the region of 2 to 256. Averaged samples are stored as 32 bit values and can be processed by any software. The trigger detection is still running with full sampling speed allowing a very precise relation between acquired signal and the trigger.

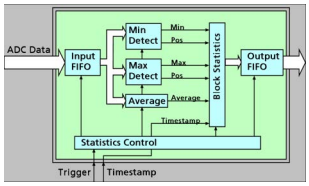
Firmware Option Block Average



The Block Average Module improves the fidelity of noisy repetitive signals. Multiple repetitive acquisitions with very small dead-time are accumulated and averaged. Random noise is reduced by the averaging process improving the visibility of the repetitive signal. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

Please see separate data sheet for details on the firmware option.

Firmware Option Block Statistics (Peak Detect)



The Block Statistics and Peak Detect Module implements a widely used data analysis and reduction technology in hardware. Each block is scanned for minimum and maximum peak and a summary including minimum, maximum, average, timestamps and position information is stored in memory. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

Please see separate data sheet for details on the firmware option.

AWG Hardware Features and Options

Singleshot output

When singleshot output is activated the data of the on-board memory is played exactly one time. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

Repeated output

When the repeated output mode is used the data of the on-board memory is played continuously for a programmed number of times or until a stop command is executed. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

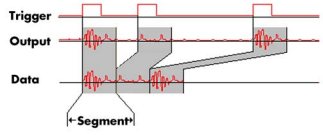
Single Restart replay

When this mode is activated the data of the on-board memory will be replayed once after each trigger event. The trigger source can be either the external TTL trigger or software trigger.

FIFO mode

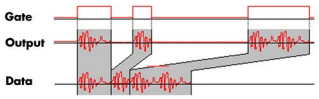
The FIFO mode is designed for continuous data transfer between PC memory or hard disk and the generation board. The control of the data stream is done automatically by the driver on an interrupt request basis. The complete installed on-board memory is used for buffering data, making the continuous streaming extremely reliable.

Multiple Replay



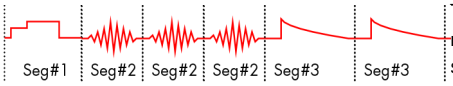
The Multiple Replay mode allows the fast output generation on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided into several segments of the same size. Each segment can contain different data which will then be played with the occurrence of each trigger event.

Gated Replay



The Gated Sampling mode allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has attained a programmed level.

Sequence Mode



The sequence mode allows to split the card memory into several data segments of different length. These data segments are chained up in a user chosen order using an additional sequence memory. In this sequence memory the number of loops for each segment can be programmed and trigger conditions can be defined to proceed from segment to segment. Using the sequence mode it is also possible to switch between replay waveforms by a simple software command or to redefine waveform data for segments simultaneously while other segments are being replayed. All trigger-related and software-command-related functions are only working on single cards, not on star-hub-synchrnonized cards.

External trigger input

All boards can be triggered using up to two external analog or digital signals. One external trigger input has two analog comparators that can define an edge or window trigger, a hysteresis trigger or a rearm trigger. The other input has one comparator that can be used for standard edge and level triggers.

hybridNETBOX Technical Data - Digitizer

Analog Inputs

Resolution	130 MS/s up to 250 MS/s 400 MS/s and 500 MS/s	16 bit (441, 442, 447, 822, 827) 14 bit (445, 448, 825, 828)	
Input Type		Single-ended	
ADC Differential non linearity (DNL)	ADC only	±0.5 LSB (14 Bit ADC), ±0.4 LSB (16 Bit ADC)	
ADC Integral non linearity (INL)	ADC only	±2.5 LSB (14 Bit ADC), ±10.0 LSB (16 Bit ADC)	
ADC Word Error Rate (WER)	max. sampling rate	10^{-12}	
Channel selection	software programmable	1, 2, or 4 (maximum is model dependent)	
Bandwidth filter	activate by software	20 MHz bandwidth with 3rd order Butterworth filtering	
Input Path Types	software programmable	**50 Ω (HF) Path**	**Buffered (high impedance) Path**
Analog Input impedance	software programmable	50 Ω	1 MΩ || 25 pF or 50 Ω
Input Ranges	software programmable	±500 mV, ±1 V, ±2.5 V, ±5 V	±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Programmable Input Offset	Frontend HW-Version < V9	not available	not available
Programmable Input Offset	Frontend HW-Version >= V9	–100%..0% on all ranges	–100%..0% on all ranges except ±1 V and ±10 V
Input Coupling	software programmable	AC/DC	AC/DC
Offset error (full speed)	after warm-up and calibration	< 0.1% of range	< 0.1% of range
Gain error (full speed)	after warm-up and calibration	< 1.0% of reading	< 1.0% of reading
Over voltage protection	range ≤ ±1V	2 Vrms	±5 V (1 MΩ), 5 Vrms (50 Ω)
Over voltage protection	range ≥ ±2V	6 Vrms	±30 V (1 MΩ), 5 Vrms (50 Ω)
Max DC voltage if AC coupling active		±30 V	±30 V
Relative input stage delay		Bandwidth filter disabled: 0 ns Bandwidth filter enabled: 14.7 ns	Bandwidth filter disabled: 3.8 ns Bandwidth filter enabled: 18.5 ns
Crosstalk 1 MHz sine signal	range ±1V	≤96 dB	≤93 dB
Crosstalk 20 MHz sine signal	range ±1V	≤82 dB	≤82 dB
Crosstalk 1 MHz sine signal	range ±5V	≤97 dB	≤85 dB
Crosstalk 20 MHz sine signal	range ±5V	≤82 dB	≤82 dB

	M4i.441x M4x.441x DN2.441-xx DN6.441-xx	M4i.442x M4x.442x DN2.442-xx DN6.442-xx DN2.822-xx	M4i.445x M4x.445x DN2.445-xx DN6.445-xx DN2.825-xx	M4i.447x M4x.447x DN2.447-xx DN6.447-xx DN2.827-xx	M4i.448x M4x.448x DN2.448-xx DN6.448-xx DN2.828-xx
lower bandwidth limit (DC coupling)	0 Hz	0 Hz	0 Hz	0 Hz	0 Hz
lower bandwidth limit (AC coupled, 50 Ω)	< 30 kHz	< 30 kHz	< 30 kHz	< 30 kHz	< 30 kHz
lower bandwidth limit (AC coupled, 1 MΩ)	< 2 Hz	< 2 Hz	< 2 Hz	< 2 Hz	< 2 Hz
-3 dB bandwidth (HF path, AC coupled, 50 Ω)	65 MHz	125 MHz	250 MHz	125 MHz	250 MHz
Flatness within ±0.5 dB (HF path, AC coupled, 50 Ω)	40 MHz	80 MHz	160 MHz	80 MHz	160 MHz
-3 dB bandwidth (Buffered path, DC coupled, 1 MΩ)	50 MHz	85 MHz	85 MHz (V1.1) 125 MHz (V1.2)	85 MHz	125 MHz (V1.2)
-3 dB bandwidth (bandwidth filter enabled)	20 MHz	20 MHz	20 MHz	20 MHz	20 MHz

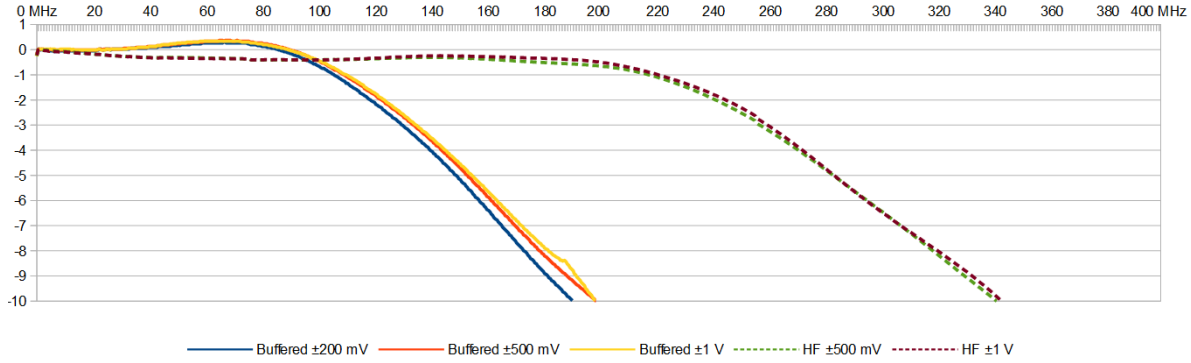
Trigger

Available trigger modes	software programmable	Channel Trigger, External, Software, Window, Re-Arm, Or/And, Delay, PXI (M4x only)	
Channel trigger level resolution	software programmable	14 bit	
Trigger engines		1 engine per channel with two individual levels, 2 external triggers	
Trigger edge	software programmable	Rising edge, falling edge or both edges	
Trigger delay	software programmable	0 to (8GSamples - 16) = 8589934576 Samples in steps of 16 samples	
Multi, Gate, ABA: re-arming time		40 samples (+ programmed pretrigger)	
Pretrigger at Multi, ABA, Gate, FIFO, Boxcar	software programmable	16 up to [8192 Samples in steps of 16)	
Posttrigger	software programmable	16 up to 8G samples in steps of 16 (defining pretrigger in standard scope mode)	
Memory depth	software programmable	32 up to [installed memory / number of active channels] samples in steps of 16	
Multiple Recording/ABA segment size, Boxcar	software programmable	32 up to [installed memory / 2 / active channels] samples in steps of 16	
Trigger accuracy (all sources)		1 sample	
Boxcar (high-resolution) average factor	software programmable	2, 4, 8, 16, 32, 64, 128 or 256	
Timestamp modes	software programmable	Standard, Startreset, external reference clock on X0 (e.g. PPS from GPS, IRIG-B)	
Data format		Std., Startreset: 64 bit counter, increments with sample clock (reset manually or on start) RefClock: 24 bit upper counter (increment with RefClock) 40 bit lower counter (increments with sample clock, reset with RefClock)	
Extra data	software programmable	none, acquisition of X0/X1/X2 inputs at trigger time, trigger source (for OR trigger)	
Size per stamp		128 bit = 16 bytes	
External trigger		**Ext0**	**Ext1**
External trigger impedance	software programmable	50 Ω /1 kΩ	1 kΩ
External trigger coupling	software programmable	AC or DC	fixed DC
External trigger type		Window comparator	Single level comparator
External input level		±10 V (1 kΩ), ±2.5 V (50 Ω),	±10 V
External trigger sensitivity (minimum required signal swing)		2.5% of full scale range	2.5% of full scale range = 0.5 V
External trigger level	software programmable	±10 V in steps of 10 mV	±10 V in steps of 10 mV
External trigger maximum voltage		±30V	±30 V

Trigger edge	software programmable	Rising edge, falling edge or both edges	
External trigger bandwidth DC	50 Ω 1 kΩ	DC to 200 MHz DC to 150 MHz	n.a. DC to 200 MHz
External trigger bandwidth AC	50 Ω	20 kHz to 200 MHz	n.a.
Minimum external trigger pulse width		≥ 2 samples	≥ 2 samples

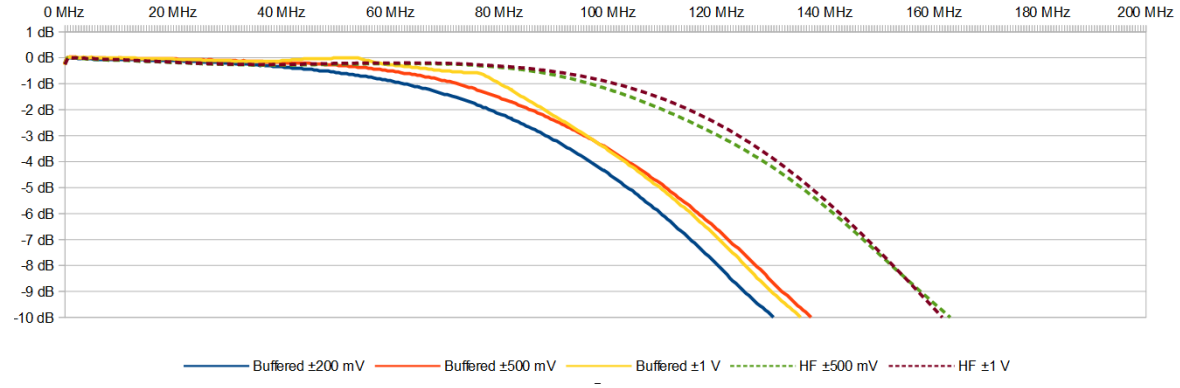
Frequency Response M4i.445x, M4x.445x, DN2.445-xx, DN6.445-xx and DN2.825-xx

Sampling Rate 500 MS/s
HF Path 50 Ω, AC coupling, no filter
Buffered Path 1 MΩ, AC Coupling, no filter



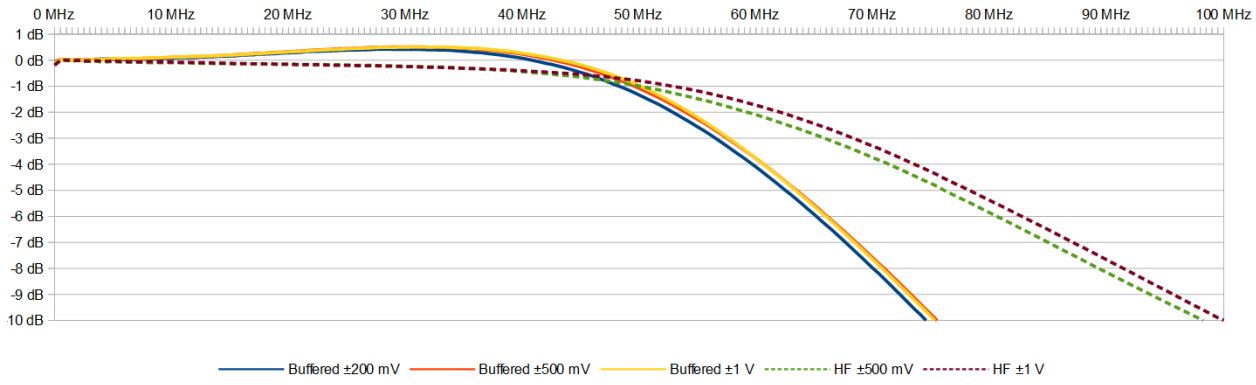
Frequency Response M4i.442x, M4x.442x, DN2.442-xx, DN6.442-xx and DN2.822-xx

Sampling Rate 250 MS/s
HF Path 50 Ω, AC coupling, no filter
Buffered Path 1 MΩ, AC Coupling, no filter



Frequency Response M4i.441x, M4x.441x, DN2.441-xx and DN6.441-xx

Sampling Rate 130 MS/s
HF Path 50 Ω, AC coupling, no filter
Buffered Path 1 MΩ, AC Coupling, no filter



Clock

Clock Modes	software programmable	internal PLL, external reference clock, Star-Hub sync (digitizerNETBOX and M4i only), PXI Reference Clock (M4x only)
Internal clock accuracy		≤ ±20 ppm
Internal clock setup granularity	standard clock mode	divider: maximum sampling rate divided by: 1, 2, 4, 8, 16, ... up to 131072 (full gain accuracy)
Internal clock setup granularity	special clock mode only	1 Hz (reduced gain accuracy when using special clock mode), only available for single cards (no star-hub), for digitizerNETBOX only available for models with one internal digitizer.
Clock setup range gaps	special clock mode only	un-setable clock speeds: 17.5 MHz to 17.9 MHz, 35.1 MHz to 35.8 MHz, 70 MHz to 72 MHz, 140 MHz to 144 MHz, 281 MHz to 287 MHz
External reference clock range	software programmable	≥ 10 MHz and ≤ 1 GHz
External reference clock input impedance		50 Ω fixed
External reference clock input coupling		AC coupling
External reference clock input edge		Rising edge
External reference clock input type		Single-ended, sine wave or square wave
External reference clock input swing	square wave	0.3 V peak-peak up to 3.0 V peak-peak
External reference clock input swing	sine wave	1.0 V peak-peak up to 3.0 V peak-peak
External reference clock input max DC voltage		±30 V (with max 3.0 V difference between low and high level)
External reference clock input duty cycle requirement		45% to 55%
Internal ADC clock output type		Single-ended, 3.3V LVPECL
Internal ADC clock output frequency	standard clock mode	Fixed to maximum sampling rate (500 MS/s, 250 MS/s or 130 MS/s depending on type)
Internal ADC clock output frequency	special clock mode	445x and 825 models (500 MS/s): ADC clock in the range between 80 MS/s and 500 MS/s 448x and 828 models (400 MS/s): ADC clock in the range between 80 MS/s and 400 MS/s 442x and 822 models (250 MS/s): ADC clock in the range between 40 MS/s and 250 MS/s 447x and 827 models (180 MS/s): ADC clock in the range between 40 MS/s and 180 MS/s 441x models (130 MS/s): ADC clock in the range between 40 MS/s and 130 MS/s
Star-Hub synchronization clock modes	software selectable	Standard clock mode with internal reference (maxmimum clock + divider), Standard clock mode with external reference (maxmimum clock + divider) special clock mode not allowed, except: 445 series (500 MS/s) can also run with 400 MS/s and divided clock for synchronization 442 series (250 MS/s) can also run with 180 MS/s and divided clock for synchronization
ABA mode clock divider for slow clock	software programmable	16 up to (128k - 16) in steps of 16
Channel to channel skew on one card		< 60 ps (typical)
Skew between star-hub synchronized cards		< 130 ps (typical, preliminary)

	M4i.441x M4x.441x DN2.441-xx DN6.441-xx	M4i.442x M4x.442x DN2.442-xx DN6.442-xx DN2.822-xx	M4i.445x M4x.445x DN2.445-xx DN6.445-xx DN2.825-xx	M4i.447x M4x.447x DN2.447-xx DN6.447-xx DN2.827-xx	M4i.448x M4x.448x DN2.448-xx DN6.448-xx DN2.828-xx
ADC Resolution	16 bit	16 bit	14 bit	16 bit	14 bit
max sampling clock	130 MS/s	250 MS/s	500 MS/s	180 MS/s	400 MS/s
min sampling clock (standard clock mode)	3.814 kS/s	3.814 kS/s	3.814 kS/s	3.814 kS/s	3.814 kS/s
min sampling clock (special clock mode)	0.610 kS/s	0.610 kS/s	0.610 kS/s	0.610 kS/s	0.610 kS/s

Block Average Signal Processing Option M4i.44xx/M4x.44xx/DN2.44x/DN6.44x/DN2.82x Series

		Firmware ≥ V1.14 (since August 2015)	**Firmware < V1.14**
Minimum Waveform Length		32 samples	32 samples
Minimum Waveform Stepsize		16 samples	16 samples
Maximum Waveform Length	1 channel active	128 kSamples	32 kSamples
Maximum Waveform Length	2 channels active	64 kSamples	16 kSamples
Maximum Waveform Length	4 or more channels active	32 kSamples	8 kSamples
Minimum Number of Averages		2	2
Maximum Number of Averages		65536 (64k)	65536 (64k)
Data Output Format	fixed	32 bit signed integer	32 bit signed integer
Re-Arming Time between waveforms		40 samples (+ programmed pretrigger)	40 samples (+ programmed pretrigger)
Re-Arming Time between end of average to start of next average		Depending on programmed segment length, max 100 µs	40 samples (+ programmed pretrigger)

Block Statistics Signal Processing Option M4i.44xx/M4x.44xx/DN2.44x/DN6.44x/DN2.82x Series

Minimum Waveform Length		32 samples
Minimum Waveform Stepsize		16 samples
Maximum Waveform Length	Standard Acquisition	2 GSamples / channels
Maximum Waveform Length	FIFO Acquisition	2 GSamples
Data Output Format	fixed	32 bytes statistics summary
Statistics Information Set per Waveform		Average, Minimum, Maximum, Position Minimum, Position Maximum, Trigger Timestamp
Re-Arming Time between Segments		40 samples (+ programmed pretrigger)

Multi Purpose I/O lines (front-plate)

Number of multi purpose lines		three, named X0, X1, X2
Input: available signal types	software programmable	Asynchronous Digital-In, Synchronous Digital-In, Timestamp Reference Clock
Input: impedance		10 kΩ to 3.3 V
Input: maximum voltage level		-0.5 V to +4.0 V
Input: signal levels		3.3 V LVTTL
Input: bandwith		125 MHz
Output: available signal types	software programmable	Asynchronous Digital-Out, Trigger Output, Run, Arm, PLL Refclock, System Clock
Output: impedance		50 Ω
Output: signal levels		3.3 V LVTTL
Output: type		3.3V LVTTL, TTL compatible for high impedance loads
Output: drive strength		Capable of driving 50 Ω loads, maximum drive strength ±48 mA
Output: update rate	14bit or 16 bit ADC resolution	sampling clock
Output: update rate	7 bit or 8 bit ADC resolution	Current sampling clock ≤ 1.25 GS/s : sampling clock Current sampling clock > 1.25 GS/s and ≤ 2.50 GS/s : ½ sampling clock Current sampling clock > 2.50 GS/s and ≤ 5.00 GS/s : ¼ sampling clock

RMS Noise Level (Zero Noise), typical figures

M4i.445x, M4x.445x, DN2.445-xx, DN6.445-xx and DN2.825-xx, 14 Bit 500 MS/s
M4i.448x, M4x.448x, DN2.448-xx, DN6.448-xx and DN2.828-xx, 14 Bit 400 MS/s

Input Range	±200 mV		±500 mV		±1		±2 V		±2.5 V		±5 V		±10 V	
Voltage resolution	24.4 µV		61.0 µV		122.1 µV		244.1 µV		305.2 µV		610.4 µV		1.22 mV	
HF path, DC, fixed 50 Ω			<1.9 LSB	<116 µV	<1.9 LSB	<232 µV			<1.9 LSB	<580 µV	<1.9 LSB	<1.16 mV		
Buffered path, full bandwidth	<3.8 LSB	<93 µV	<2.7 LSB	<165 µV	<2.1 LSB	<256 µV	<3.8 LSB	<928 µV			<2.7 LSB	<1.65 mV	<2.0 LSB	<2.44 mV
Buffered path, BW limit active	<2.2 LSB	<54 µV	<2.0 LSB	<122 µV	<2.0 LSB	<244 µV	<3.2 LSB	<781 µV			<2.3 LSB	<1.40 mV	<2.0 LSB	<2.44 mV

M4i.442x, M4x.442x, DN2.442-xx, DN6.442-xx and DN2.822-xx, 16 Bit 250 MS/s
M4i.447x, M4x.447x, DN2.447-xx, DN6.447-xx and DN2.827-xx, 16 Bit 180 MS/s

Input Range	±200 mV		±500 mV		±1		±2 V		±2.5 V		±5 V		±10 V	
Voltage resolution	6.1 µV		15.3 µV		30.5 µV		61.0 µV		76.3 µV		152.6 µV		305.2 µV	
HF path, DC, fixed 50 Ω			<6.9 LSB	<53 µV	<6.9 LSB	<211 µV			<6.9 LSB	<526 µV	<6.9 LSB	<1.05 mV		
Buffered path, full bandwidth	<11 LSB	<67 µV	<7.8 LSB	<119 µV	<7.1 LSB	<217 µV	<12 LSB	<732 µV			<8.1 LSB	<1.24 mV	<7.1 LSB	<2.17 mV
Buffered path, BW limit active	<7.9 LSB	<48 µV	<7.0 LSB	<107 µV	<6.9 LSB	<211 µV	<9.8 LSB	<598 µV			<7.2 LSB	<1.10 mV	<7.1 LSB	<2.17 mV

M4i.441x, M4x.441x, DN2.441-xx and DN6.441-xx, 16 Bit 130 MS/s

Input Range	±200 mV		±500 mV		±1		±2 V		±2.5 V		±5 V		±10 V	
Voltage resolution (1)	6.1 µV		15.3 µV		30.5 µV		61.0 µV		76.3 µV		152.6 µV		305.2 µV	
HF path, DC, fixed 50 Ω			<5.9 LSB	<90 µV	<5.9 LSB	<180 µV			<5.9 LSB	<450 µV	<5.9 LSB	<900 µV		
Buffered path, full bandwidth	<8.5 LSB	<52 µV	<6.5 LSB	<99 µV	<5.9 LSB	<180 µV	<11 LSB	<671 µV			<7.0 LSB	<1.07 mV	<6.1 LSB	<1.86 mV
Buffered path, BW limit active	<7.0 LSB	<43 µV	<6.1 LSB	<93 µV	<5.9 LSB	<180 µV	<9.6 LSB	<586 µV			<6.7 LSB	<1.02 mV	<6.1 LSB	<1.86 mV

Dynamic Parameters

M4i.445x, M4x.445x, DN2.445-xx, DN6.445-xx and DN2.825-xx, 14 Bit 500 MS/s
M4i.448x, M4x.448x, DN2.448-xx, DN6.448-xx and DN2.828-xx, 14 Bit 400 MS/s

Input Path	HF path, AC coupled, fixed 50 Ohm						Buffered path, BW limit			Buffered path, full BW		
Test signal frequency	10 MHz				40 MHz	70 MHz	10 MHz			10 MHz	40 MHz	70 MHz
Input Range	±500mV	±1V	±2.5V	±5V	±1V	±1V	±200mV	±500mV	±1V	±500mV	±500mV	±500mV
THD (typ) (dB	<-75.9 dB	<-75.8 dB	<-75.2 dB	<-74.8 dB	<-72.5 dB	<-67.4 dB	<-71.4 dB	<-72.1 dB	<-68.6 dB	<-65.0 dB	<-58.6 dB	<-54.4 dB
SNR (typ) (dB)	>67.8 dB	>67.9 dB	>68.0 dB	>68.0 dB	>69.5 dB	>67.5 dB	>67.5 dB	>68.0 dB	>68.1 dB	>67.3 dB	>65.8 dB	>65.6 dB
SFDR (typ), excl. harm. (dB)	>88.1 dB	>88.6 dB	>85.2 dB	>85.3 dB	>88.0 dB	>87.8 dB	>87.3 dB	>88.4 dB	>87.5 dB	>89.0 dB	>88.9 dB	>88.8 dB
SFDR (typ), incl. harm. (dB)	>80.1 dB	>80.0 dB	>77.4 dB	>77.3 dB	>74.0 dB	>69.9 dB	>78.1 dB	>73.5 dB	>69.8 dB	>67.5 dB	>60.8 dB	>56.0 dB
SINAD/THD+N (typ) (dB)	>67.2 dB	>67.2 dB	>67.2 dB	>67.2 dB	>67.7 dB	>64.4 dB	>66.5 dB	>66.6 dB	>65.3 dB	>63.9 dB	>57.9 dB	>54.0 dB
ENOB based on SINAD (bit)	>10.9 bit	>10.9 bit	>10.9 bit	>10.9 bit	>10.9 bit	>10.4 bit	>10.7 bit	>10.8 bit	>10.6 bit	>10.3 bit	>9.3 bit	>8.7 bit
ENOB based on SNR (bit)	>11.0 bit	>11.0 bit	>11.0 bit	>11.0 bit	>11.0 bit	>10.9 bit	>10.9 bit	>11.0 bit	>11.0 bit	>10.9 bit	>10.6 bit	>10.6 bit

M4i.442x, M4x.442x, DN2.442-xx, DN6.442-xx and DN2.822-xx, 16 Bit 250 MS/s
M4i.447x, M4x.447x, DN2.447-xx, DN6.447-xx and DN2.827-xx, 16 Bit 180 MS/s

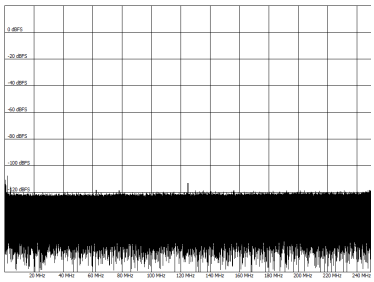
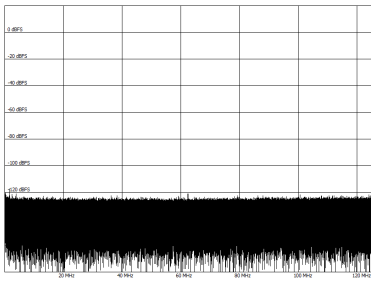
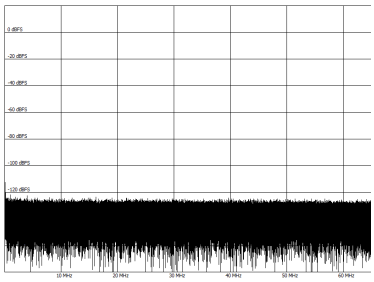
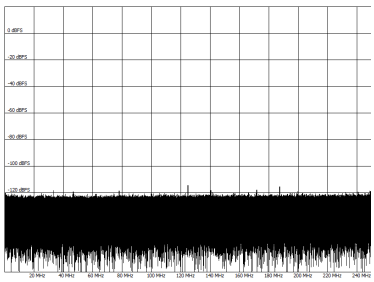
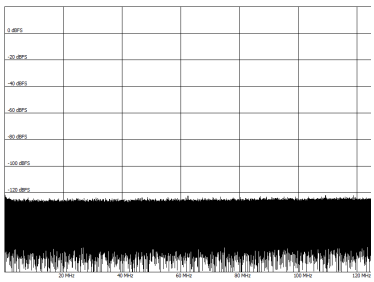
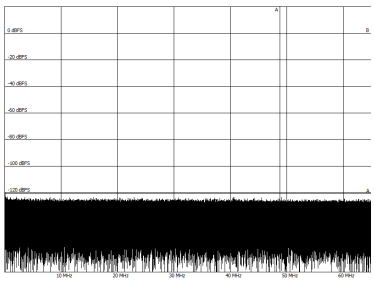
Input Path	HF path, AC coupled, fixed 50 Ohm						Buffered path, BW limit			Buffered path, full BW		
Test signal frequency	1 MHz	10 MHz				40 MHz	10 MHz			1 MHz	10 MHz	40 MHz
Input Range	±1V	±500mV	±1V	±2.5V	±5V	±1V	±200mV	±500mV	±1V	±500mV	±500mV	±500mV
THD (typ) (dB	<-73.1 dB	<-74.0 dB	<-74.1 dB	<-74.1 dB	<-74.1 dB	<-62.9 dB	<-73.2 dB	<-71.5 dB	<-69.0 dB	<-72.2 dB	<-67.5 dB	<49.8 dB
SNR (typ) (dB)	>71.9 dB	>71.5 dB	>71.5 dB	>71.6 dB	>71.6 dB	>71.8 dB	>69.8 dB	>71.0 dB	>71.2 dB	>71.7 dB	>71.0 dB	>69.0 dB
SFDR (typ), excl. harm. (dB)	>92.1 dB	>90.4 dB	>90.8 dB	>90.1 dB	>89.7 dB	>90.2 dB	>92.1 dB	>92.0 dB	>92.1 dB	>90.0 dB	>91.4 dB	>92.5 dB
SFDR (typ), incl. harm. (dB)	>74.4 dB	>75.4 dB	>75.5 dB	>75.5 dB	>75.5 dB	>64.5 dB	>75.0 dB	>73.1 dB	>69.8 dB	>74.7 dB	>67.8 dB	>50.0 dB
SINAD/THD+N (typ) (dB)	>69.8 dB	>69.6 dB	>69.6 dB	>69.6 dB	>69.6 dB	>62.2 dB	>68.5 dB	>68.2 dB	>67.0 dB	>68.8 dB	>66.4 dB	>48.9 dB
ENOB based on SINAD (bit)	>11.3 bit	>11.2 bit	>11.2 bit	>11.3 bit	>11.3 bit	>10.0 bit	>11.1 bit	>11.0 bit	>10.8 bit	>11.1 dB	>10.7 bit	>7.8 bit
ENOB based on SNR (bit)	>11.7 bit	>11.6 bit	>11.6 bit	>11.6 bit	>11.6 bit	>11.6 dB	>11.3 bit	>11.5 bit	>11.5 bit	>11.6 dB	>11.5 bit	>11.2 bit

M4i.441x, M4x.441x, DN2.441-xx and DN6.441-xx, 16 Bit 130 MS/s

Input Path	HF path, AC coupled, fixed 50 Ohm						Buffered path, BW limit			Buffered path, full BW		
Test signal frequency	1 MHz	10 MHz					10 MHz			1 MHz	10 MHz	
Input Range	±1V	±500mV	±1V	±2.5V	±5V		±200mV	±500mV	±1V	±500mV	±500mV	
THD (typ) (dB	<-72.6 dB	<-77.8 dB	<-77.5 dB	<-77.3 dB	<-77.1 dB		<-74.5 dB	<-73.9 dB	<-70.1 dB	<-73.5 dB	<73.4 dB	
SNR (typ) (dB)	>72.2 dB	>71.8 dB	>71.9 dB	>72.0 dB	>72.0 dB		>69.8 dB	>71.2 dB	>71.3 dB	>71.1 dB	>71.0 dB	
SFDR (typ), excl. harm. (dB)	>92.4 dB	>97.0 dB	>96.0 dB	>95.2 dB	>94.8 dB		>89.0 dB	>94.0 dB	>94.5 dB	>88.8 dB	>93.5 dB	
SFDR (typ), incl. harm. (dB)	>73.7 dB	>78.6 dB	>78.2 dB	>75.2 dB	>75.1 dB		>77.6 dB	>77.8 dB	>71.5 dB	>74.7 dB	>73.1 dB	
SINAD/THD+N (typ) (dB)	>69.4 dB	>70.8 dB	>70.8 dB	>70.9 dB	>70.8 dB		>69.0 dB	>69.7 dB	>68.2 dB	>69.2 dB	>69.2 dB	
ENOB based on SINAD (bit)	>11.2 bit	>11.5 bit	>11.5 bit	>11.5 bit	>11.5 bit		>11.2 bit	>11.3 bit	>11.0 bit	>11.2 bit	>11.2 bit	
ENOB based on SNR (bit)	>11.7 bit	>11.6 bit	>11.6 bit	>11.6 bit	>11.6 bit		>11.3 bit	>11.5 bit	>11.5 bit	>11.6 bit	>11.6 bit	

Dynamic parameters are measured at ±1 V input range (if no other range is stated) and 50Ω termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave generated by a signal generator and a matching bandpass filter. Amplitude is >99% of FSR. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits.

Noise Floor Plots (open inputs)

	M4i.445x, M4x.445x, DN2.445-xx, DN6.445-xx, DN2.825-xx Sampling Rate 500 MS/s	**M4i.442x, M4x.442x, DN2.442-xx , DN6.442-xx, DN2.822-xx** Sampling Rate 250 MS/s	**M4i.441x, M4x.441x, DN2.441-xx, DN6.441-xx** Sampling Rate 130 MS/s
Buffered Path 1 MΩ, AC ±1 V range			
HF Path 50 Ω, AC ±500 mV			

hybridNETBOX Technical Data - Arbitrary Waveform Generator

Analog Outputs

Resolution		16 bit
D/A Interpolation		no interpolation

		M4i.662x/M4x.662x DN2.662/DN6.662x DN2.82x-04	M4i.663x/M4x.663x DN2.663/DN6.663 DN2.82x-02	high bandwidth version (1.25 GS/s + option -hbw)
Output amplitude into 50 Ω termination	software programmable	±80 mV up to ±2.5 V	±80 mV up to ±2 V	±80 mV up to ±480 mV
Output amplitude into high impedance loads	software programmable	±160 mV up to ±5 V	±160 mV up to ±4 V	±160 mV up to ±960 mV
Stepsize of output amplitude (50 Ω termination)		1 mV	1 mV	1 mV
Stepsize of output amplitude (high impedance)		2 mV	2 mV	2 mV
10% to 90% rise/fall time of 480 mV pulse			1.06 ns	440 ps
10% to 90% rise/fall time of 2000 mV pulse			1.08 ns	n.a.

Output offset	fixed	0 V
Output Amplifier Path Selection	automatically by driver	Low Power path: ±80 mV to ±480 mV (into 50 Ω) High Power path: ±420 mV to ±2.5 V/±2 V (into 50 Ω)
Output Amplifier Setting Hysteresis	automatically by driver	420 mV to 480 mV (if output is using low power path it will switch to high power path at 480 mV. If output is using high power path it will switch to low power path at 420 mV)
Output amplifier path switching time		10 ms (output disabled while switching)
Filters	software programmable	bypass with no filter or one fixed filter
DAC Differential non linearity (DNL)	DAC only	±0.5 LSB typical
DAC Integral non linearity (INL)	DAC only	±1.0 LSB typical
Output resistance		50 Ω
Minimum output load		0 Ω (short circuit safe)
Output accuracy	Low power path High power path	±0.5 mV ±0.1% of programmed output amplitude ±1.0 mV ±0.2% of programmed output amplitude

Trigger

Available trigger modes	software programmable	External, Software, Window, Re-Arm, Or/And, Delay, PXI (M4x only)
Trigger edge	software programmable	Rising edge, falling edge or both edges
Trigger delay	software programmable	0 to (8GSamples - 32) = 8589934560 Samples in steps of 32 samples
Multi, Gate: re-arming time		40 samples
Trigger to Output Delay	sample rate ≤ 625 MS/s sample rate > 625 MS/s	238.5 sample clocks + 16 ns 476.5 sample clocks + 16 ns
Memory depth	software programmable	32 up to [installed memory / number of active channels] samples in steps of 32
Multiple Replay segment size	software programmable	16 up to [installed memory / 2 / active channels] samples in steps of 16
Trigger accuracy (all sources)		1 sample
Minimum external trigger pulse width		≥ 2 samples

External trigger		**Ext0**	**Ext1**
External trigger impedance	software programmable	50 Ω /1 kΩ	1 kΩ
External trigger coupling	software programmable	AC or DC	fixed DC
External trigger type		Window comparator	Single level comparator
External input level		±10 V (1 kΩ), ±2.5 V (50 Ω),	±10 V
External trigger sensitivity (minimum required signal swing)		2.5% of full scale range	2.5% of full scale range = 0.5 V
External trigger level	software programmable	±10 V in steps of 10 mV	±10 V in steps of 10 mV
External trigger maximum voltage		±30V	±30 V
External trigger bandwidth DC	50 Ω 1 kΩ	DC to 200 MHz DC to 150 MHz	n.a. DC to 200 MHz
External trigger bandwidth AC	50 Ω	20 kHz to 200 MHz	n.a.
Minimum external trigger pulse width		≥ 2 samples	≥ 2 samples

Multi Purpose I/O lines (front-plate)

Number of multi purpose lines		three, named X0, X1, X2
Input: available signal types	software programmable	Asynchronous Digital-In
Input: impedance		10 kΩ to 3.3 V
Input: maximum voltage level		-0.5 V to +4.0 V
Input: signal levels		3.3 V LVTTL
Output: available signal types	software programmable	Asynchronous Digital-Out, Synchronous Digital-Out, Trigger Output, Run, Arm, Marker Output, System Clock
Output: impedance		50 Ω
Output: signal levels		3.3 V LVTTL
Output: type		3.3V LVTTL, TTL compatible for high impedance loads
Output: drive strength		Capable of driving 50 Ω loads, maximum drive strength ±48 mA
Output: update rate		sampling clock

Sequence Replay Mode (Mode available starting with firmware V1.14)

Number of sequence steps	software programmable	1 up to 4096 (sequence steps can be overloaded at runtime)
Number of memory segments	software programmable	2 up to 64k (segment data can be overloaded at runtime)
Minimum segment size	software programmable	384 samples (1 active channel), 192 samples (2 active channels), 96 samples (4 active channels), in steps of 32 samples.
Maximum segment size	software programmable	2 GS / active channels / number of sequence segments (round up to the next power of two)
Loop Count	software programmable	1 to (1M - 1) loops
Sequence Step Commands	software programmable	Loop for #Loops, Next, Loop until Trigger, End Sequence
Special Commands	software programmable	Data Overload at runtime, sequence steps overload at runtime, readout current replayed sequence step
Limitations for synchronized products		Software commands changing the sequence as well as „Loop until trigger" are not synchronized between cards. This also applies to multiple AWG modules in a generatorNETBOX.

Clock

Clock Modes	software programmable	internal PLL, external reference clock, Star-Hub sync (generatorNETBOX and M4i only), PXI Reference Clock (M4x only)
Internal clock accuracy		≤ ±20 ppm
Internal clock setup granularity		8 Hz (internal reference clock only, restrictions apply to external reference clock)
Setable Clock speeds		50 MHz to max sampling clock
Clock Setting Gaps		750 to 757 MHz, 1125 to 1145 MHz (no sampling clock possible in these gaps)
External reference clock range	software programmable	≥ 10 MHz and ≤ 1.25 GHz
External reference clock input impedance		50 Ω fixed
External reference clock input coupling		AC coupling
External reference clock input edge		Rising edge
External reference clock input type		Single-ended, sine wave or square wave
External reference clock input swing	square wave	0.3 V peak-peak up to 3.0 V peak-peak
External reference clock input swing	sine wave	1.0 V peak-peak up to 3.0 V peak-peak
External reference clock input max DC voltage		±30 V (with max 3.0 V difference between low and high level)
External reference clock input duty cycle requirement		45% to 55%
External reference clock output type		Single-ended, 3.3V LVPECL
Clock output	sampling clock ≤71.68 MHz	Clock output = sampling clock/4
Clock output	sampling clock >71.68 MHz	Clock output = sampling clock/8
Star-Hub synchronization clock modes	software selectable	Internal clock, external reference clock

Bandwidth and Slewrate

	Filter	**Output Amplitude**	**M4i.663x-x8 M4x.663x-x8 DN2.663-xx DN6.663-xx DN2.82x-02**	**M4i.662x-x8 M4x.662x-x8 DN2.662-xx DN6.662-xx DN2.82x-04**
Maximum Output Rate			1.25 GS/s	625 MS/s
-3dB Bandwidth	no Filter	±480 mV	400 MHz	200 MHz
-3dB Bandwidth	no Filter	±1000 mV	320 MHz	200 MHz
-3dB Bandwidth	no Filter	±2000 mV	320 MHz	200 MHz
-3dB Bandwidth	Filter	all	65 MHz	65 MHz
Slewrate	no Filter	±480 mV	4.5 V/ns	2.25 V/ns

Dynamic Parameters

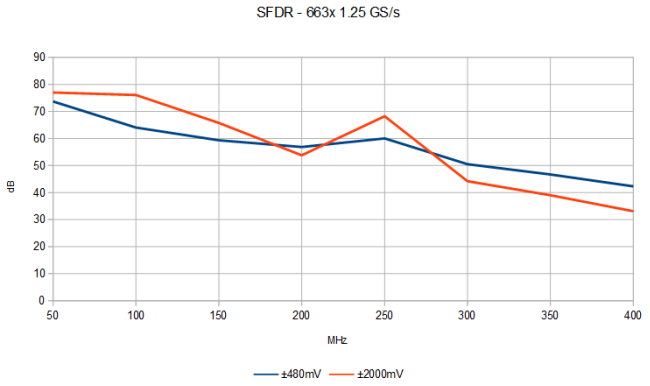
	M4i.662x-x8 M4x.662x-x8 DN2.662-xx DN6.662-xx DN2.82x-04						
Test - Samplerate	625 MS/s			625 MS/s		625 MS/s	
Output Frequency	10 MHz			50 MHz		50 MHz	
Output Level in 50 Ω	±480 mV	±1000mV	±2500mV	±480 mV	±2500mV	±480 mV	±2500mV
Used Filter	none			none		Filter enabled	
NSD (typ)	-150 dBm/Hz	-149 dBm/Hz	-149 dBm/Hz	-150 dBm/Hz	-149 dBm/Hz	-150 dBm/Hz	-149 dBm/Hz
SNR (typ)	70.7 dB	72.4 dB	63.1 dB	65.3 dB	64.4 dB	67.5 dB	69.4 dB
THD (typ)	-73.3 dB	-70.5 dB	-49.7 dB	-64.1 dB	-39.1 dB	-68.4 dB	-50.4 dB
SINAD (typ)	69.0 dB	67.7 dB	49.5 dB	61.6 dB	39.1 dB	64.9 dB	50.3 dB
SFDR (typ), excl harm.	98 dB	98 dB	99 dB	86 dB	76 dB	88 dB	89 dB
ENOB (SINAD)	11.2	11.0	8.0	10.0	6.2	10.5	8.1
ENOB (SNR)	11.5	11.7	10.2	10.5	10.4	10.9	11.2

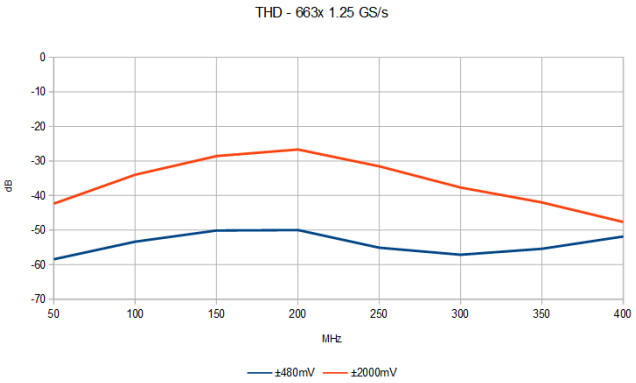
	M4i.663x-x8 M4x.663x-x8 DN2.663-xx DN6.663-xx DN2.82x-02						
Test - Samplerate	1.25 GS/s			1.25 GS/s		1.25 GS/s	
Output Frequency	10 MHz			50 MHz		50 MHz	
Output Level in 50 Ω	±480 mV	±1000mV	±2000mV	±480 mV	±2000mV	±480 mV	±2000mV
Used Filter	none			none		Filter enabled	

	M4i.663x-x8 M4x.663x-x8 DN2.663-xx DN6.663-xx DN2.82x-02						
NSD (typ)	-150 dBm/Hz	-149 dBm/Hz	-149 dBm/Hz	-150 dBm/Hz	-149 dBm/Hz	-150 dBm/Hz	-149 dBm/Hz
SNR (typ)	70.5 dB	72.1 dB	71.4 dB	65.2 dB	65.0 dB	67.2 dB	68.2 dB
THD (typ)	-74.5 dB	-73.5 dB	-59.1 dB	-60.9 dB	-43.9 dB	-67.9 dB	-63.1 dB
SINAD (typ)	69.3 dB	69.7 dB	59 dB	59.5 dB	43.9 dB	64.5 dB	61.9 dB
SFDR (typ), excl harm.	96 dB	97 dB	98 dB	85 dB	84 dB	87 dB	87 dB
ENOB (SINAD)	11.2	11.2	9.5	9.6	6.9	10.4	10.0
ENOB (SNR)	11.5	11.5	11.5	10.5	10.5	10.9	11.0

THD and SFDR are measured at the given output level and 50 Ohm termination with a high resolution M3i.4860/M4i.4450-x8 data acquisition card and are calculated from the spectrum. Noise Spectral Density is measured with built-in calculation from an HP E4401B Spectrum Analyzer. All available D/A channels are activated for the tests. SNR and SFDR figures may differ depending on the quality of the used PC. NSD = Noise Spectral Density, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range.

SFDR and THD versus signal frequency





- Measurements done with a spectrum analyzer bandwidth of 1.5 GHz
- Please note that the bandwidth of the high range output is limited to 320 MHz
- Please note that the output bandwidth limit also affects the THD as harmonics higher than the bandwidth are filtered

hybridNETBOX Technical Data - General

Connectors

Analog Channels		SMA female (one for each single-ended input)	Cable-Type: Cab-3mA-xx-xx
Clock Input		SMA female	Cable-Type: Cab-3mA-xx-xx
Clock Output		SMA female	Cable-Type: Cab-3mA-xx-xx
Trg0 Input		SMA female	Cable-Type: Cab-3mA-xx-xx
Trg1 Input		SMA female	Cable-Type: Cab-3mAxx-xx
X0/Trigger Output/Timestamp Reference Clock	programmable direction	SMA female	Cable-Type: Cab-3mA-xx-xx
X1	programmable direction	SMA female	Cable-Type: Cab-3mA-xx-xx
X2	programmable direction	SMA female	Cable-Type: Cab-3mA-xx-xx

Option digitizerNETBOX/generatorNETBOX embedded server (DN2.xxx-Emb, DN6.xxx-Emb)

CPU	Intel Quad Core 2 GHz	
System memory	4 GByte RAM	
System data storage	Internal 128 GByte SSD	
Development access	Remote Linux command shell (ssh), no graphical interface (GUI) available	
Accessible Hardware	Full access to Spectrum instruments, LAN, front panel LEDs, RAM, SSD	
Integrated operating system	OpenSuse 12.2 with kernel 4.4.7.	
Internal PCIe connection	DN2.20, DN2.46, DN2.47, DN2.49, DN2.59, DN2.60, DN2.65 DN6.46, DN6.49, DN6.59, DN6.65, DN2.80, DN2.81	PCIe x1, Gen1
	DN2.22, DN2.44, DN2.66 DN6.22, DN6.44, DN6.66, DN2.82	PCIe x1, Gen2

Ethernet specific details

LAN Connection		Standard RJ45	
LAN Speed		Auto Sensing: GBit Ethernet, 100BASE-T, 10BASE-T	
LAN IP address	programmable	DHCP (IPv4) with AutoIP fall-back (169.254.x.y), fixed IP (IPv4)	
Sustained Streaming speed		DN2.20, DN2.46, DN2.47, DN2.49, DN2.60 DN6.46, DN6.49	up to 70 MByte/s
		DN2.59, DN2.65, DN2.22, DN2.44, DN2.66 DN6.59, DN6.65, DN6.22, DN6.44, DN6.66	up to 100 MByte/s
Used TCP/UDP Ports		Webserver: 80 VISA Discovery Protocol: 111, 9757 Spectrum Remote Server: 1026, 5025	mDNS Daemon: 5353 UPNP Daemon: 1900

Power connection details

Mains AC power supply	Input voltage: 100 to 240 VAC, 50 to 60 Hz
AC power supply connector	IEC 60320-1-C14 (PC standard coupler)
Power supply cord	power cord included for Schuko contact (CEE 7/7)

Serial connection details (DN2.xxx with hardware ≥ V11)

Serial connection (RS232)	For diagnostic purposes only. Do not use, unless being instructed by a Spectrum support agent.

Certification, Compliance, Warranty

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark
Product warranty	5 years starting with the day of delivery
Software and firmware updates	Life-time, free of charge

DN2 specific Technical Data

Environmental and Physical Details DN2.xxx

Dimension of Chassis without connectors or bumpers	L x W x H	366 mm x 267 mm x 87 mm
Dimension of Chassis with 19" rack mount option	L x W x H	366 mm x 482.6 mm x 87 mm (2U height)
Weight (1 internal acquisition/generation module)		6.3 kg, with rack mount kit: 6.8 kg
Weight (2 internal acquisition/generation modules)		6.7 kg, with rack mount kit 7.2 kg
Warm up time		20 minutes
Operating temperature		0°C to 40°C
Storage temperature		-10°C to 70°C
Humidity		10% to 90%
Dimension of packing (single DN2)	L x W x H	470 mm x 390 mm x 180 mm
Volume weight of Packing (single DN2)		7.0 kgs

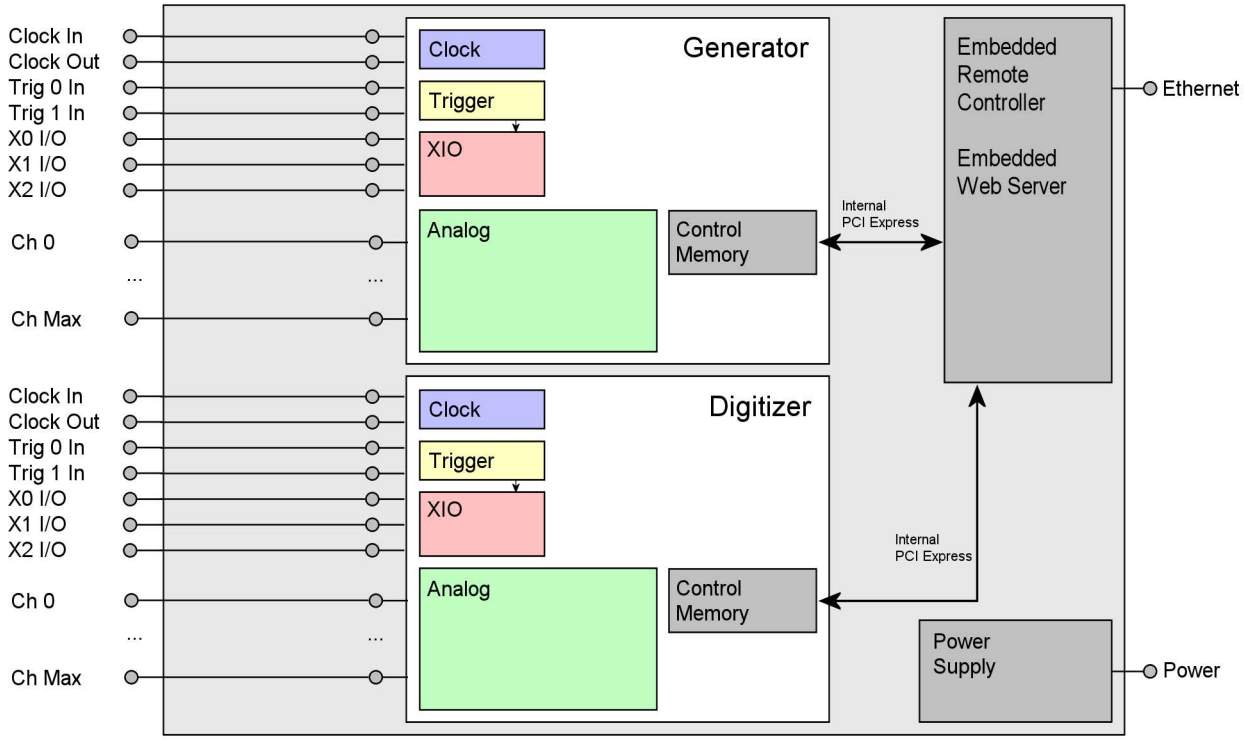
Power Consumption

	230 VAC	12 VDC	24 VDC
2 + 2 channel versions			
4 + 4 channel versions			

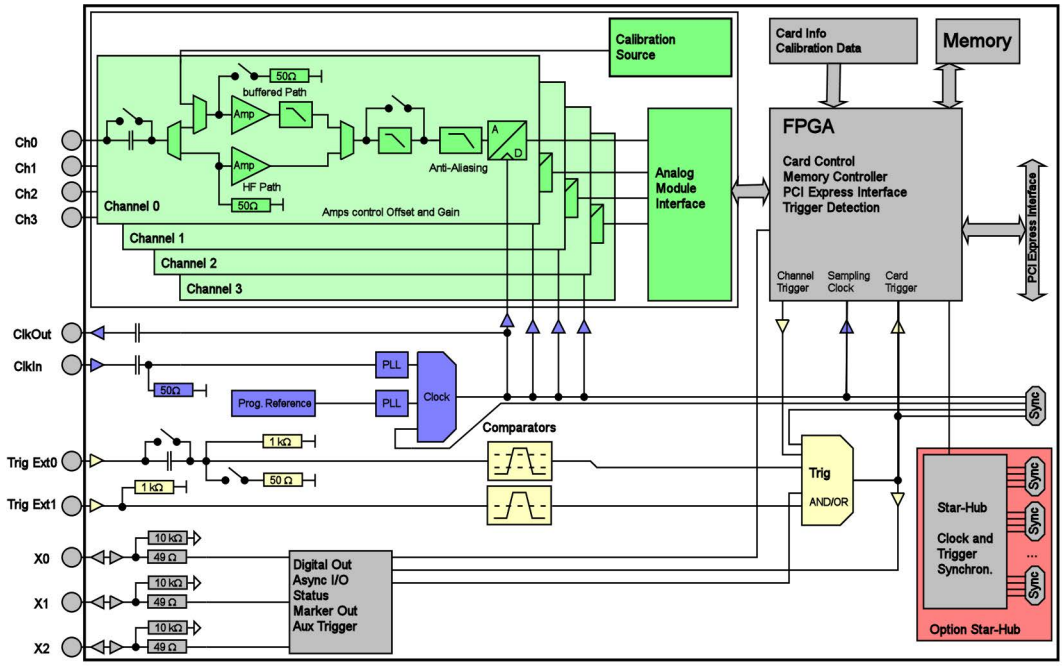
MTBF

MTBF	TBD

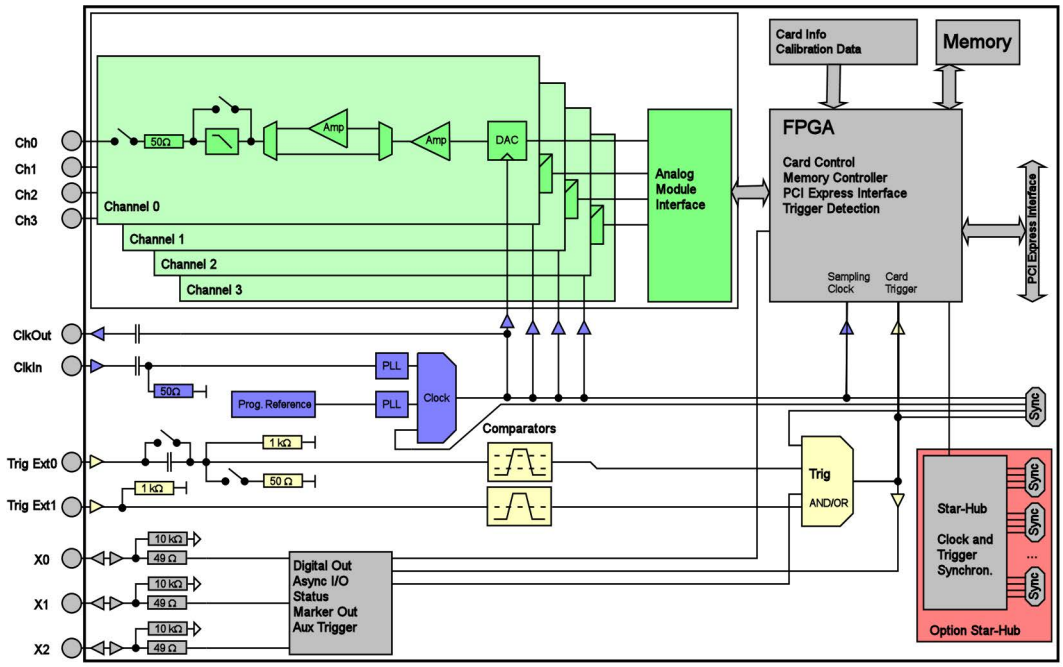
Block diagram of hybridNETBOX DN2



Block diagram of Digitizer Module inside hybridNETBOX DN2.82x



Block diagram of AWG Module inside hybridNETBOX DN2.82x



Order Information

The hybridNETBOX is equipped with a large internal memory for data storage and data replay. The internal digitizer supports standard acquisition (Scope), FIFO acquisition (streaming), Multiple Recording, Gated Sampling, ABA mode and Timestamps. Then internal AWG supports standard replay, FIFO replay (streaming), Multiple Replay, Gated Replay, Continuous Replay (Loop), Single-Restart as well as Sequence. Operating system drivers for Windows/Linux 32 bit and 64 bit, drivers and examples for C/C++, IVI (Scope, Digitizer and Function Generator class), LabVIEW (Windows), MATLAB (Windows and Linux), .NET, Delphi, Java, Python, Julia and a Professional license of the oscilloscope software SBench 6 are included.

The system is delivered with a connection cable meeting your countries power connection. Additional power connections with other standards are available as option.

hybridNETBOX DN2 - Ethernet/LXI Interface

		Digitizer		AWG			
Order no.	Memory	Resolution	Speed	Resolution	Speed	Level@50Ω	Level@1MΩ
DN2.822-02	2 x 2 GSamples	16 Bit	2 x 250 MS/s	16 Bit	2 x 1.25 GS/s	±2.0 V	±4.0 V
DN2.822-04	2 x 2 GSamples	16 Bit	4 x 250 MS/s	16 Bit	4 x 625 MS/s	±2.5 V	±5.0 V
DN2.825-02	2 x 2 GSamples	14 Bit	2 x 500 MS/s	16 Bit	2 x 1.25 GS/s	±2.0 V	±4.0 V
DN2.825-04	2 x 2 GSamples	14 Bit	4 x 500 MS/s	16 Bit	4 x 625 MS/s	±2.5 V	±5.0 V
DN2.827-02[1]	2 x 2 GSamples	16 Bit	2 x 180 MS/s	16 Bit	2 x 1.25 GS/s	±2.0 V	±4.0 V
DN2.827-04[1]	2 x 2 GSamples	16 Bit	4 x 180 MS/s	16 Bit	4 x 625 MS/s	±2.5 V	±5.0 V
DN2.828-02[1]	2 x 2 GSamples	14 Bit	2 x 400 MS/s	16 Bit	2 x 1.25 GS/s	±2.0 V	±4.0 V
DN2.828-04[1]	2 x 2 GSamples	14 Bit	4 x 400 MS/s	16 Bit	4 x 625 MS/s	±2.5 V	±5.0 V

[1]Export Version

Options

Order no.	Option
DN2.xxx-Rack	19" rack mounting set for self mounting
DN2.xxx-Emb	Extension to Embedded Server: CPU, more memory, SSD. Access via remote Linux secure shell (ssh)
DN2.xxx-spavg	Signal Processing Firmware Option: Block Average (later installation by firmware - upgrade available)
DN2.xxx-spstat	Signal Processing Firmware Option: Block Statistics/Peak Detect (later installation by firmware - upgrade available)
DN2.xxx-DC12	12 VDC internal power supply. Replaces AC power supply. Accepts 9 V to 18 V DC input. Screw terminals.
DN2.xxx-DC24	24 VDC internal power supply. Replaces AC power supply. Accepts 18 V to 36 V DC input. Screw terminals
DN2.xxx-BTPWR	Boot on Power On: the digitizerNETBOX/generatorNETBOX automatically boots if power is switched on.

Services

Order no.	Option
DN2.xxx-Recal	Recalibration of complete digitizerNETBOX/generatorNETBOX DN2 including calibration protocol

Standard SMA Cables

The standard adapter cables are based on RG174 cables and have a nominal attenuation of 0.3 dB/m at 100 MHz and 0.5 dB/m at 250 MHz. For high speed signals we recommend the low loss cables series CHF.

for Connections	Connection	Length	to BNC male	to BNC female	to SMB female	to MMCX male	to SMA male	
All	SMA male	80 cm	Cab-3mA-9m-80	Cab-3mA-9f-80	Cab-3f-3mA-80	Cab-1m-3mA-80	Cab-3mA-3mA-80	
All	SMA male	200 cm	Cab-3mA-9m-200	Cab-3mA-9f-200	Cab-3f-3mA-200	Cab-1m-3mA-200	Cab-3mA-3mA-200	
Probes (short)	SMA male	5 cm		Cab-3mA-9f-5				

Low Loss SMA Cables

The low loss adapter cables are based on MF141 cables and have an attenuation of 0.3 dB/m at 500 MHz and 0.5 dB/m at 1.5 GHz. They are recommended for signal frequencies of 200 MHz and above.

Order no.	Option
CHF-3mA-3mA-200	Low loss cables SMA male to SMA male 200 cm
CHF-3mA-9m-200	Low loss cables SMA male to BNC male 200 cm

Technical changes and printing errors possible